4GSPS / 2GSPS / 1GSPS 12b Analog-To-Digital Converter (ADC)

1 Characteristics

- Resolution: 12-bit, NO missing code
- Sampling Rate:
  CAE2500 : 4 GSPS (single) , 2 GSPS (dual)
  CAE2600 : 2 GSPS (single) , 1 GSPS (dual)
  CAE2700 : 1 GSPS (single) , 0.5 GSPS (dual)
- # Channels: 1 or 2
- Input Signal Range [$V_{pp,diff}$]: 0.8V (typ) , 1V (max)
- Analog Input Bandwidth (-3dB): 3.0 GHz
- Code error rate: < 10^{-15}
- Integral-Nonlinearity INL :
  CAE2500 : -1.3 / +1.3 LSB @ 180 MHz
  CAE2600 : -0.5 / +0.5 LSB @ 110 MHz
  CAE2700 : -0.7 / +0.7 LSB @ 110 MHz
- Differential-Nonlinearity DNL :
  CAE2500 : -0.32 / +0.40 LSB @ 180 MHz
  CAE2600 : -0.37 / +0.37 LSB @ 110 MHz
  CAE2700 : +0.28 / -0.28 LSB @ 110 MHz
- SNR @ -1 dBFS :
  CAE2500 : 52.1 dBFS (0.8V_{pp}), 53.6 dBFS (1.0V_{pp})
  CAE2600 : 55.1 dBFS (1V_{pp})
  CAE2700 : 55.4 dBFS (1V_{pp})
- SFDR @ -1 dBFS :
  CAE2500 : 75.8 dBFS (0.8V_{pp}), 74.4 dBFS (1.0V_{pp})
  CAE2600 : 77.2 dBFS (1V_{pp})
  CAE2700 : 77.9 dBFS (1V_{pp})
- ENOB @ -1 dBFS :
  CAE2500 : 8.4b (0.8V_{pp}), 8.6b (1.0V_{pp})
  CAE2600 : 8.8b (1V_{pp})
  CAE2700 : 8.9b (1V_{pp})
- 16 lanes JESD204B output, with maximum lane rate of 10.0 Gbps, support 8b/10b coding, and support subclass 1
- Embedded Programmable DDC: Programmable FIR banks with decimation ratio of 1x,2x,3x,4x,6x,8x, 12x,16x,24x,32x,48x, and 64x for real output, or with decimation ratio of 2x,4x,6x,8x,16x,24x,32x, 48x,64x,96x,128x for complex I/Q output.
  The 48-bit NCO is embedded in each DDC and support fast frequency hopping
- Clamp diode protection in analog differential input
- Temperature-Tracked diode embedded
- Junction temperature: -40 to 115°C
- Low Power Consumption:
  CAE2500 : 1.9W (single) , 2.0W (dual)
  CAE2600 : 1.66W (single) , 1.75W (dual)
  CAE2700 : 1.36W (single) , 1.40W (dual)
- Package: FCBGA196 (12mm x 12mm)

2 Applications

- Oscilloscope and Wideband digitizer
- Broadband communications
- High-Speed Data Acquisition Unit
- Communication Tester (802.11ad, 5G)
- Wireless Software Defined Ratio (SDR)
- Spectrometer

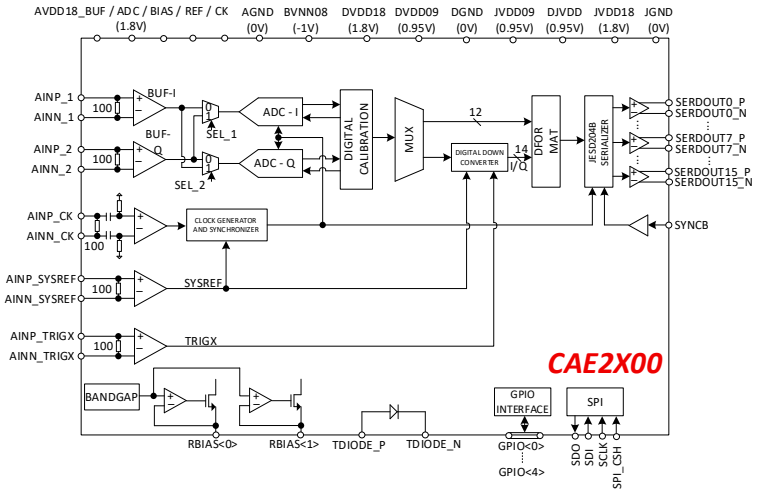
3 General Descriptions

CAE2500 / CAE2600 / CAE2700 is a 12b RF Analog-To-Digital Converter (ADC) with maximum sampling rate of 4GSPS / 2GSPS / 1GSPS in single channel mode, and with maximum sampling rate of 2GSPS / 1GSPS / 0.5GSPS in dual channel mode.

The single or dual channel mode can be configured by SPI setting, can be developed by flexible hardware to support multi-channels or wide instantaneous bandwidth applications.

CAE2500 / CAE2600 / CAE2700 adopt high speed JESD204B output interface, with the operating junction temperature of -40 to 115°C, and the package of Flip-Chip BGA 196 pins (12mm x 12mm).

4 Functional Block Diagram

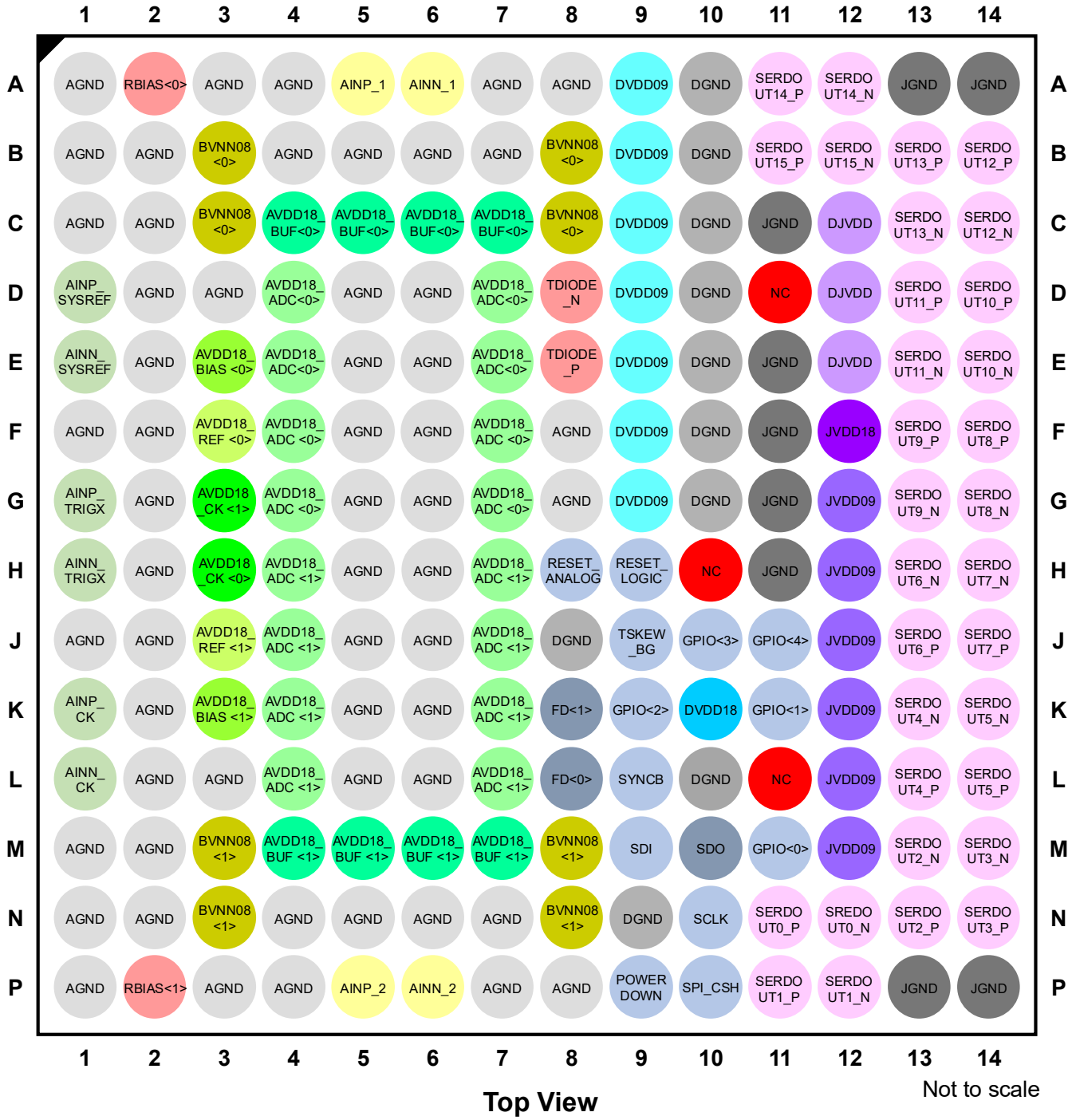


Outline

5 Edition History

Date	Version	Contents Updated
2026.1	Rev 1.1 Eng	First Draft

6 Pin Configuration and Functions



Top View

Not to scale

Fig 6-1. 196-Ball Flip Chip BGA

Table 6-1. Pin Functions

Pin Number	Pin Name	Type	Descriptions
A2 P2	RBIAS<0> RBIAS<1>	Input	These pins are used to generate internal reference current bias for analog circuits. Each pin is required to connect a 12k ohm resistor to ground with 0.1% accuracy and Tempco of 25ppm/°C below.
A5	AINP_1	Input	Dual Channel Mode：Positive Analog Input Terminal of I-channel Single Channel Mode：Positive of Analog Input Terminal (Default Input) This pin is internally connected to 50-ohm resistor (single-ended), it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. The pin is the default positive analog input terminal in single channel mode.
A6	AINN_1	Input	Dual Channel Mode：Negative Analog Input Terminal of I-channel Single Channel Mode：Negative of Analog Input Terminal (Default Input) This pin is internally connected to 50-ohm resistor (single-ended), it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. The pin is the default negative analog input terminal in single channel mode.
P5	AINP_2	Input	Dual Channel Mode：Positive Analog Input Terminal of Q-channel Single Channel Mode：Positive of Analog Input Terminal (SPI Sets) This pin is internally connected to 50-ohm resistor (single-ended), it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. The pin can be configured as the positive analog input terminal in single channel mode by SPI set.
P6	AINN_2	Input	Dual Channel Mode：Negative Analog Input Terminal of Q-channel Single Channel Mode：Negative of Analog Input Terminal (SPI Sets) This pin is internally connected to 50-ohm resistor (single-ended), it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. The pin can be configured as the negative analog input terminal in single channel mode by SPI set.
D1	AINP_SYSREF	Input	Differential SYSREF Signal（Positive） It is internally connected a 50-ohm resistor (single-ended), and it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. This pin is used to align data timing for multi-chip purpose.
E1	AINN_SYSREF	Input	Differential SYSREF Signal（Negative） It is internally connected a 50-ohm resistor (single-ended), and it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. This pin is used to align data timing for multi-chip purpose.
G1	AINP_TRIGX	Input	Differential Trigger X Signal (Positive) It is internally connected a 50-ohm resistor (single-ended), and it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. This pin is used to synchronize NCO of DDC.
H1	AINN_TRIGX	Input	Differential Trigger X Signal (Negative) It is internally connected a 50-ohm resistor (single-ended), and it allows either DC or AC coupled. Notice that the applied DC common mode is required to fulfil the range of input common mode shown in Section 7. This pin is used to synchronize NCO of DDC.
K1	AINP_CK	Input	Differential Main Clock Signal (Positive) Although it is internally connected a 50-ohm resistor (single-ended) with internal AC coupled, the applied DC common mode is required to fulfil the range of input common mode shown in Section 7 to maximize the swing. This pin is used to provide the main clock of the chip.
L1	AINN_CK	Input	Differential Main Clock Signal (Negative) Although it is internally connected a 50-ohm resistor (single-ended) with internal AC coupled, the applied DC common mode is required to fulfil the range of input common mode shown in Section 7 to maximize the swing. This pin is used to provide the main clock of the chip.

Table 6-2. Pin Functions (Continued)

Pin Number	Pin Name	Type	Descriptions
E8	TDIODE_P	Input	Temperature Diode Connection (Positive) It is used to connect an external temperature sensor to monitor the temperature of internal chip. If it is unused, please leave it floating.
D8	TDIODE_N	Input	Temperature Diode Connection (Negative) It is used to connect an external temperature sensor to monitor the temperature of internal chip. If it is unused, please leave it floating.
B3, B8, C3, C8 M3, M8, N3, N8	BVNN08<0> BVNN08<1>	Input	Negative Analog Supply Pins It is required to connect to negative LDO, and to satisfy the requirement of the specifications on DC level and current sink.
C4, C5, C6, C7 M4,M5, M6, M7	AVDD18_BUF<0> AVDD18_BUF<1>	Input	1.8V Power Supply of Analog Input Buffer
E3 K3	AVDD18_BIAS<0> AVDD18_BIAS<1>	Input	1.8V Power Supply of Analog Bias Circuitry
D4, D7, E4, E7, F4, F7, G4, G7 H4, H7, J4, J7, K4, K7, L4, L7	AVDD18_ADC<0> AVDD18_ADC<1>	Input	1.8V Power Supply of Core ADC Circuitry
F3 J3	AVDD18_REF<0> AVDD18_REF<1>	Input	1.8V Power Supply of Reference Buffer Circuitry
H3 G3	AVDD18_CK<0> AVDD18_CK<1>	Input	1.8V Power Supply of Clock Generator Circuitry
A1, A3, A4, A7, A8, B1, B2, B4, B5, B6, B7, C1, C2, D2, D3, D5, D6, E2, E5, E6, F1, F2, F5, F6, F8, G2, G5, G6, G8, H2, H5, H6, J1, J2, J5, J6, K2, K5, K6, L2, L3, L5, L6, M1, M2, N1, N2, N4, N5, N6, N7, P1, P3, P4, P7, P8	AGND	Input	Analog Ground
A9, B9, C9, D9, E9, F9, G9	DVDD09	Input	0.95V Digital Core Power Supply
K10	DVDD18	Input	1.8V Digital I/O Power Supply
A10, B10, C10, D10, E10, F10, J8, N9, G10, L10,	DGND	Input	Digital Ground
H8	RESET_ANALOG	Input	This pin is to reset of analog circuitry when main clock is applied with logic high for reset and logic low for normal operation (1.8V logic)
H9	RESET_LOGIC	Input	This pin is to hard reset of digital circuitry with logic high for reset and logic low for normal operation (1.8V logic). When digital power-on, internal POR will automatically reset all digital circuits. It can be ignored and kept logic 0 if it is unused
L8 K8	FD<0> FD<1>	Output	These pins are used to track the power level of the input signal. with FD<0> for I-channel and FD<1> for Q-channel (1.8V logic)
J9	TSKEW_BG	Input	This pin allows external FPGA or processor to enable the background timing skew calibration during normal operation with active high (1.8V logic)
L9	SYNCB	Input	JESD204B Synchronized signal， with logic low during RX/TX synchronization of JESD204B interface and logic high for completion of the process (1.8V logic)

Table 6-3. Pin Functions (Continued)

Pin Number	Pin Name	Type	Descriptions
J11 J0 K9 K11 M11	GPIO<4> GPIO<3> GPIO<2> GPIO<1> GPIO<0>	Input	These pins are used to perform fast frequency hopping of NCO in embedded DDC (1.8V logic)
P10	SPI_CSH	Input	Chip select of SPI, with active 1 during SPI read/write and active 0 during SPI reset (1.8V logic)
N10	SCLK	Input	SPI Clock Input (1.8V logic)
M9	SDI	Input	SPI Data Input (1.8V logic)
M10	SDO	Output	SPI Data Output (1.8V logic)
P9	POWERDOWN	Input	External Power down of Chip with logic 1 for power-down and logic 0 for normal operation (1.8V logic)
D11, H10, L11	NC	/	No Connection, Floating, those pins are not allowed to either logic 1 or 0
C12, D12, E12	DJVDD	Input	0.95V JESD204B Core Digital Power Supply
G12, H12, J12, K12, L12, M12	JVDD09	Input	0.95V JESD204B SerDes Power Supply
F12	JVDD18	Input	1.8V JESD204B Digital I/O Power Supply
A13, A14, C11, E11, F11, G11, H11, P13, P14	JGND	Input	JESD204B Ground
N11 N12	SERDOUT0_P SERDOUT0_N	Output	Lane 0 Differential Serdes Output, with 100-ohm differential resistor connected
P11 P12	SERDOUT1_P SERDOUT1_N	Output	Lane 1 Differential Serdes Output, with 100-ohm differential resistor connected
N13 M13	SERDOUT2_P SERDOUT2_N	Output	Lane 2 Differential Serdes Output, with 100-ohm differential resistor connected
N14 M14	SERDOUT3_P SERDOUT3_N	Output	Lane 3 Differential Serdes Output, with 100-ohm differential resistor connected
L13 K13	SERDOUT4_P SERDOUT4_N	Output	Lane 4 Differential Serdes Output, with 100-ohm differential resistor connected
L14 K14	SERDOUT5_P SERDOUT5_N	Output	Lane 5 Differential Serdes Output, with 100-ohm differential resistor connected
J13 H13	SERDOUT6_P SERDOUT6_N	Output	Lane 6 Differential Serdes Output, with 100-ohm differential resistor connected
J14 H14	SERDOUT7_P SERDOUT7_N	Output	Lane 7 Differential Serdes Output, with 100-ohm differential resistor connected
F14 G14	SERDOUT8_P SERDOUT8_N	Output	Lane 8 Differential Serdes Output, with 100-ohm differential resistor connected
F13 G13	SERDOUT9_P SERDOUT9_N	Output	Lane 9 Differential Serdes Output, with 100-ohm differential resistor connected
D14 E14	SERDOUT10_P SERDOUT10_N	Output	Lane 10 Differential Serdes Output, with 100-ohm differential resistor connected
D13 E13	SERDOUT11_P SERDOUT11_N	Output	Lane 11 Differential Serdes Output, with 100-ohm differential resistor connected
B14 C14	SERDOUT12_P SERDOUT12_N	Output	Lane 12 Differential Serdes Output, with 100-ohm differential resistor connected
B13 C13	SERDOUT13_P SERDOUT13_N	Output	Lane 13 Differential Serdes Output, with 100-ohm differential resistor connected
A11 A12	SERDOUT14_P SERDOUT14_N	Output	Lane 14 Differential Serdes Output, with 100-ohm differential resistor connected
B11 B12	SERDOUT15_P SERDOUT15_N	Output	Lane 15 Differential Serdes Output, with 100-ohm differential resistor connected

7 Specifications

7.1 Electrical Characteristics

7.1.1 *CAE2500 Specifications*

Parameter	Conditions	CAE2500			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		3.0		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			2.0	GHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		12.5	31.25	MHz
Pulse Width	Burst and Periodic modes	500			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±1.3		LSB
DNL	(no missing code)		±0.4		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2500 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 4 GSPS*	CAE2500			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		52.1		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		52.1		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		53.6		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		53.5		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		51.5		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		51.7		
	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		52.8		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		53.1		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		50.4		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		51.0		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		51.4		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		52.1		
SINAD	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		52.1		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		52.1		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		53.5		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		53.5		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		51.4		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		51.7		
	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		52.7		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		53.1		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		50.4		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		50.9		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		51.3		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		52.0		
SFDR	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		75.8		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		76.4		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		74.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		72.2		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		71.0		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		72.0		
	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		69.9		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		75.5		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		69.0		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		70.8		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		68.6		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		70.5		

CAE2500 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 4 GSPS*	CAE2500			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		-83.4		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		-92.5		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		-85.8		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		-90.7		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-78.5		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		-80.7		
	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		-76.6		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		-79.3		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		-90.3		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		-89.8		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		-96.9		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		-89.8		
HD3	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		-77.6		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		-79.4		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		-74.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		-76.7		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-72.1		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		-79.3		
	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		-69.9		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		-78.5		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		-78.3		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		-73.9		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		-75.2		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		-74.3		
ENOB	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		8.4		Bit
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		8.4		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		8.6		Bit
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		8.6		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		8.3		Bit
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		8.3		
	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		8.5		Bit
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		8.5		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		8.1		Bit
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		8.2		Bit
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		8.4		

CAE2500 Specifications (Continued)

Parameter	Conditions	CAE2500			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 180MHz, -1 dBFS (1Vpp FS)		-146.6		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		4		GSPS
	Dual-Channel		2		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.25	5.0	10.0	Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		785		mA
	Normal mode, all background calibrations enable & DDC off (dual)		835		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		520		mA
Current (1.8V supplies)	Power down		26		mA
Current (0.95V supplies)	Power down		10		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		1.9		W
	Normal mode, all background calibrations enable && DDC off (dual)		2.0		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.1.2 *CAE2600 Specifications*

Parameter	Conditions	CAE2600			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		3.0		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			1.0	GHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		6.25	15.625	MHz
Pulse Width	Burst and Periodic modes	1000			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±0.5		LSB
DNL	(no missing code)		±0.37		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2600 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 2 GSPS*	CAE2600			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		55.1		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		55.1		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		55.0		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		55.2		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		54.6		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		54.8		
	Fin = 650MHz, -1.0 dBFS (1Vpp FS)		54.3		dBFS
	Fin = 650MHz, -3.0 dBFS (1Vpp FS)		54.6		
	Fin = 800MHz, -1.0 dBFS (1Vpp FS)		54.2		dBFS
	Fin = 800MHz, -3.0 dBFS (1Vpp FS)		54.5		
	Fin = 900MHz, -1.0 dBFS (1Vpp FS)		53.6		dBFS
	Fin = 900MHz, -3.0 dBFS (1Vpp FS)		54.1		
SINAD	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		55.0		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		55.1		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		54.9		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		55.1		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		54.4		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		54.8		
	Fin = 650MHz, -1.0 dBFS (1Vpp FS)		54.1		dBFS
	Fin = 650MHz, -3.0 dBFS (1Vpp FS)		54.4		
	Fin = 800MHz, -1.0 dBFS (1Vpp FS)		53.7		dBFS
	Fin = 800MHz, -3.0 dBFS (1Vpp FS)		54.3		
	Fin = 900MHz, -1.0 dBFS (1Vpp FS)		53.5		dBFS
	Fin = 900MHz, -3.0 dBFS (1Vpp FS)		54.0		
SFDR	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		77.2		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		78.2		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		74.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		77.4		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		70.0		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		76.4		
	Fin = 650MHz, -1.0 dBFS (1Vpp FS)		68.3		dBFS
	Fin = 650MHz, -3.0 dBFS (1Vpp FS)		73.7		
	Fin = 800MHz, -1.0 dBFS (1Vpp FS)		70.5		dBFS
	Fin = 800MHz, -3.0 dBFS (1Vpp FS)		73.2		
	Fin = 900MHz, -1.0 dBFS (1Vpp FS)		70.0		dBFS
	Fin = 900MHz, -3.0 dBFS (1Vpp FS)		72.1		

CAE2600 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 2 GSPS*	CAE2600			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		-91.0		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		-106.5		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		-82.6		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		-86.0		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		-79.4		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		-78.7		
	Fin = 650MHz, -1.0 dBFS (1Vpp FS)		-80.6		dBFS
	Fin = 650MHz, -3.0 dBFS (1Vpp FS)		-75.6		
	Fin = 800MHz, -1.0 dBFS (1Vpp FS)		-76.3		dBFS
	Fin = 800MHz, -3.0 dBFS (1Vpp FS)		-78.6		
	Fin = 900MHz, -1.0 dBFS (1Vpp FS)		-71.2		dBFS
	Fin = 900MHz, -3.0 dBFS (1Vpp FS)		-73.7		
HD3	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		-81.6		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		-92.8		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		-74.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		-81.0		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		-70.8		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		-77.8		
	Fin = 650MHz, -1.0 dBFS (1Vpp FS)		-68.4		dBFS
	Fin = 650MHz, -3.0 dBFS (1Vpp FS)		-72.8		
	Fin = 800MHz, -1.0 dBFS (1Vpp FS)		-70.5		dBFS
	Fin = 800MHz, -3.0 dBFS (1Vpp FS)		-77.1		
	Fin = 900MHz, -1.0 dBFS (1Vpp FS)		-86.7		dBFS
	Fin = 900MHz, -3.0 dBFS (1Vpp FS)		-89.5		
ENOB	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		8.8		Bit
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		8.9		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		8.8		Bit
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		8.9		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		8.7		Bit
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		8.8		
	Fin = 650MHz, -1.0 dBFS (1Vpp FS)		8.7		Bit
	Fin = 650MHz, -3.0 dBFS (1Vpp FS)		8.8		
	Fin = 800MHz, -1.0 dBFS (1Vpp FS)		8.6		Bit
	Fin = 800MHz, -3.0 dBFS (1Vpp FS)		8.7		
	Fin = 900MHz, -1.0 dBFS (1Vpp FS)		8.6		Bit
	Fin = 900MHz, -3.0 dBFS (1Vpp FS)		8.7		

CAE2600 Specifications (Continued)

Parameter	Conditions	CAE2600			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 110MHz, -1 dBFS (1Vpp FS)		-145.1		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		2.0		GSPS
	Dual-Channel		1.0		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.25	2.5		Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		705		mA
	Normal mode, all background calibrations enable & DDC off (dual)		755		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		412		mA
Current (1.8V supplies)	Power down		26		mA
Current (0.95V supplies)	Power down		10		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		1.66		W
	Normal mode, all background calibrations enable & DDC off (dual)		1.75		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.1.3 CAE2700 Specifications

Parameter	Conditions	CAE2700			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		3.0		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			500	MHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		3.125	7.8125	MHz
Pulse Width	Burst and Periodic modes	2000			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±0.7		LSB
DNL	(no missing code)		±0.28		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2700 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 1 GSPS*	CAE2700			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		55.4		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		55.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 300MHz, -1.0 dBFS (1Vpp FS)		55.3		dBFS
	Fin = 300MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 400MHz, -1.0 dBFS (1Vpp FS)		55.2		dBFS
	Fin = 400MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		55.2		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		55.3		
SINAD	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		55.4		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		55.3		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 300MHz, -1.0 dBFS (1Vpp FS)		55.2		dBFS
	Fin = 300MHz, -3.0 dBFS (1Vpp FS)		55.3		
	Fin = 400MHz, -1.0 dBFS (1Vpp FS)		55.2		dBFS
	Fin = 400MHz, -3.0 dBFS (1Vpp FS)		55.4		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		55.1		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		55.3		
SFDR	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		77.9		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		77.5		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		76.5		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		77.3		
	Fin = 300MHz, -1.0 dBFS (1Vpp FS)		75.1		dBFS
	Fin = 300MHz, -3.0 dBFS (1Vpp FS)		75.1		
	Fin = 400MHz, -1.0 dBFS (1Vpp FS)		75.5		dBFS
	Fin = 400MHz, -3.0 dBFS (1Vpp FS)		77.3		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		76.2		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		76.5		

CAE2700 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 1 GSPS*	CAE2700			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		-91.9		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		-95.9		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		-83.8		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		-92.3		
	Fin = 300MHz, -1.0 dBFS (1Vpp FS)		-79.9		dBFS
	Fin = 300MHz, -3.0 dBFS (1Vpp FS)		-84.8		
	Fin = 400MHz, -1.0 dBFS (1Vpp FS)		-88.6		dBFS
	Fin = 400MHz, -3.0 dBFS (1Vpp FS)		-88.4		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		-76.2		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		-76.5		
HD3	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		-83.8		dBFS
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		-86.2		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		-77.2		dBFS
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		-83.8		
	Fin = 300MHz, -1.0 dBFS (1Vpp FS)		-75.4		dBFS
	Fin = 300MHz, -3.0 dBFS (1Vpp FS)		-84.2		
	Fin = 400MHz, -1.0 dBFS (1Vpp FS)		-85.6		dBFS
	Fin = 400MHz, -3.0 dBFS (1Vpp FS)		-92.4		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		-76.5		dBFS
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		-84.4		
ENOB	Fin = 110MHz, -1.0 dBFS (1Vpp FS)		8.9		Bit
	Fin = 110MHz, -3.0 dBFS (1Vpp FS)		8.9		
	Fin = 180MHz, -1.0 dBFS (1Vpp FS)		8.9		Bit
	Fin = 180MHz, -3.0 dBFS (1Vpp FS)		8.9		
	Fin = 300MHz, -1.0 dBFS (1Vpp FS)		8.9		Bit
	Fin = 300MHz, -3.0 dBFS (1Vpp FS)		8.9		
	Fin = 400MHz, -1.0 dBFS (1Vpp FS)		8.9		Bit
	Fin = 400MHz, -3.0 dBFS (1Vpp FS)		8.9		
	Fin = 480MHz, -1.0 dBFS (1Vpp FS)		8.9		Bit
	Fin = 480MHz, -3.0 dBFS (1Vpp FS)		8.9		

CAE2700 Specifications (Continued)

Parameter	Conditions	CAE2700			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 110MHz, -1 dBFS (1Vpp FS)		-142.4		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		1.0		GSPS
	Dual-Channel		0.5		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination		1.25		Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		565		mA
	Normal mode, all background calibrations enable & DDC off (dual)		587		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		365		mA
Current (1.8V supplies)	Power down		26		mA
Current (0.95V supplies)	Power down		10		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		1.36		W
	Normal mode, all background calibrations enable & DDC off (dual)		1.40		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.2 Timing Requirements

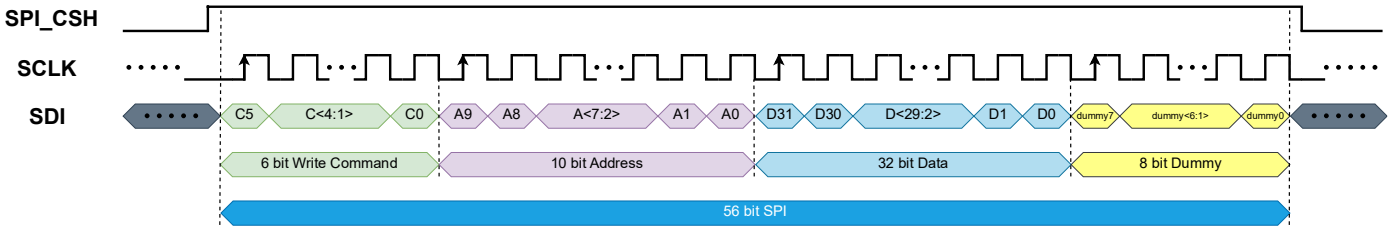


Fig 7-1. SPI Write Timing Diagram

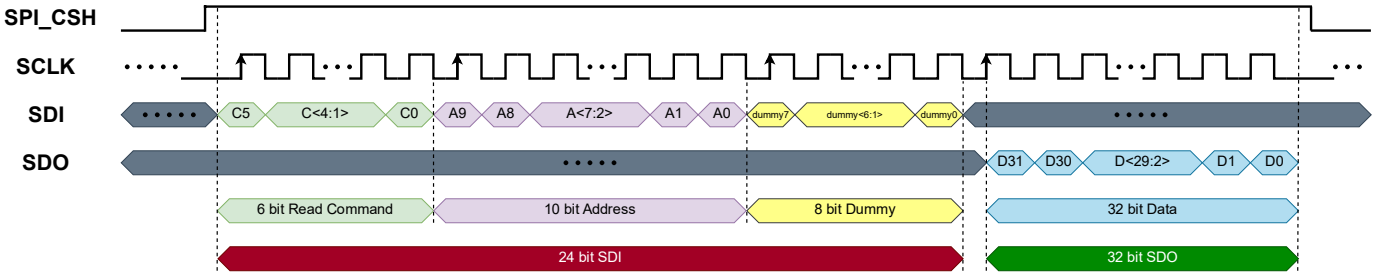


Fig 7-2. SPI Read Timing Diagram

The device features a standard 4-wire SPI interface for register configuration and JESD204B link control, supporting both internal SPI registers and JESD204B APB-mapped registers.

SPI_CSH (Chip Select) is an **active-high** signal:

- The device is selected (enabled for SPI transactions) when **SPI_CSH = 1** (logic high).
- The device is deselected (SPI interface disabled, outputs tri-stated where applicable) when **SPI_CSH = 0** (logic low).
- After chip reset (power-on reset or soft reset), **SPI_CSH** defaults to logic **1** (active / selected state by default). However, to ensure no unintended transactions occur post-reset, the master should drive **SPI_CSH** low during reset assertion and only bring it high when initiating a valid transfer.

Note: This active-high polarity is non-standard compared to the conventional active-low Chip Select used in most SPI peripherals. The master controller must configure its GPIO or SPI hardware accordingly (e.g., invert polarity if using a standard active-low driver).

All SPI transactions use a fixed **56-bit** frame format:

- Bits [55:50]: 6-bit command field (MSB first)
- Bits [49:40]: 10-bit address field
- Bits [39:0]: 40-bit data field

Command codes:

- 6'b0001_00 → Write register (SPI or APB)
- 6'b0010_00 → Read register (SPI or APB)

Address decoding:

- Addresses with MSB = 0 (0x_xxxx_xxxx) → Internal SPI configuration registers
- Addresses with MSB = 1 (1x_xxxx_xxxx) → JESD204B APB registers

SPI Write Transaction Example

Write to internal SPI register at address 10'h001 with data 32'h14183102:

- Command: 6'b0001_00
- Address: 10'b00_0000_0001
- Data: 32'h14183102 (byte order: 14 18 31 02)
- Padding: 8'b0000_0000 (dummy bits on SDI)

Timing sequence (56 SCLK cycles total):

1. First 6 SCLK: SDI = 000100 (write command)
2. Next 10 SCLK: SDI = 0000000001 (address 001h)
3. Next 32 SCLK: SDI = 00010100 00011000 00110001 00000010 (data)
4. Final 8 SCLK: SDI = 00000000 (dummy, ignored)

SPI_CSH must be held high (active) throughout the entire 56-bit transaction. After completion, the master may drive **SPI_CSH** low to deselect the device.

SPI Read Transaction Example

Read from internal SPI register at address 10'h000:

- Command: 6'b0010_00
- Address: 10'b00_0000_0000
- Dummy (TX): 8'b0000_0000 (turn-around)
- Dummy (RX padding): 32'b0...0 (SDI = 0 during readback)

Timing sequence:

1. First 6 SCLK: SDI = 001000 (read command)
2. Next 10 SCLK: SDI = 0000000000 (address 000h)
3. Next 8 SCLK: SDI = 00000000 (dummy cycles for device to prepare data)
4. Final 32 SCLK: SDI = all 0 (master dummy); device drives read data on **SDO**

SPI_CSH held high during the transaction.

Clocking and Edge Definitions

- Master changes SDI on **SCLK falling edge**
- Device samples SDI on **SCLK rising edge**
- Device updates SDO on **SCLK rising edge**
- Master samples SDO on **SCLK falling edge**

JESD204B APB Register Access

APB registers are accessed using the same 56-bit frame when address MSB = 1.

Example: APB Write to address 10'h204 with 8-bit data 8'h80:

- Command: 6'b0001_00
- Address: 10'b10_0000_0100
- Data[39:32]: 8'h80
- Data[31:0]: 32'h00000000 (dummy)

Example: APB Read from address 10'h204:

- Command: 6'b0010_00
- Address: 10'b10_0000_0100
- Dummy TX: 8'b00000000
- Read data: Returned in bits [39:32] on SDO (next 8 bits after dummy)
- Remaining: 24'b0...0 (dummy padding)

7.3 Typical Performance (AC coupled)

CAE2500
(Single Channel Mode)

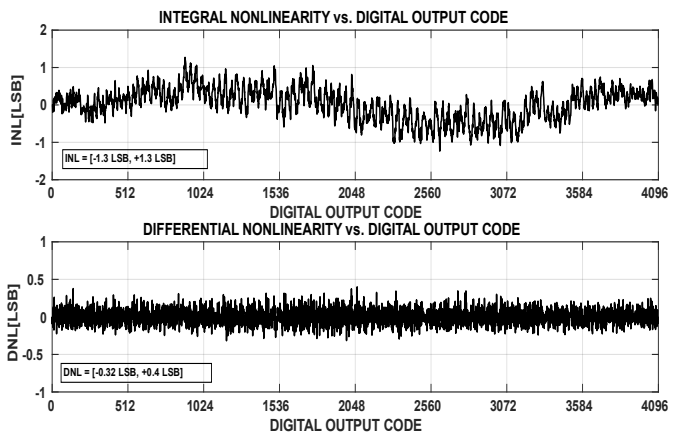


Fig 7-3. INL/DNL at Fin = 180MHz , 4GSPS (0.8Vpp FS)

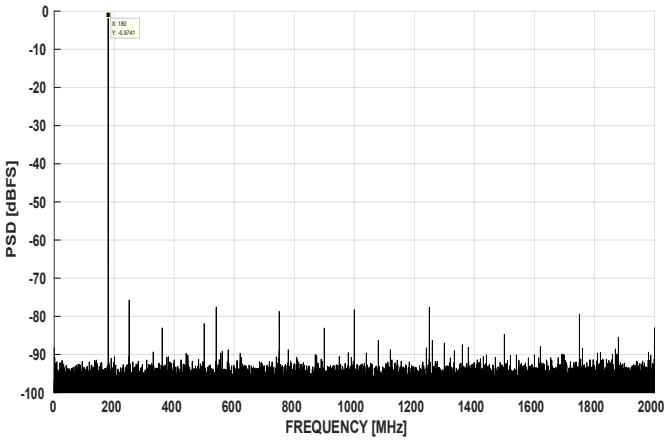


Fig 7-4. FFT at Fin = 180MHz, 4GSPS (0.8Vpp FS)

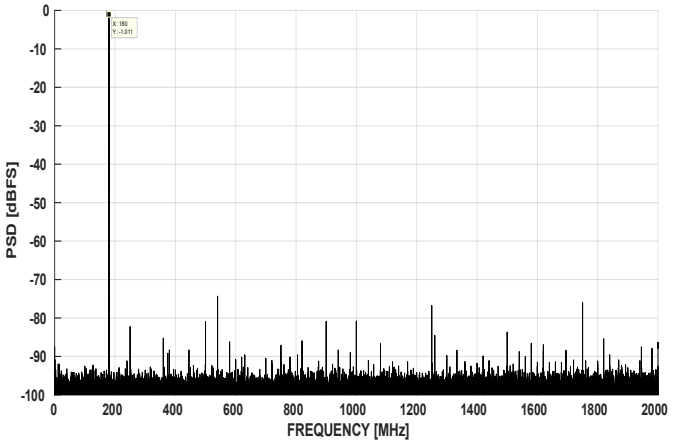


Fig 7-5.FFT at Fin = 180MHz, 4GSPS (1.0Vpp FS)

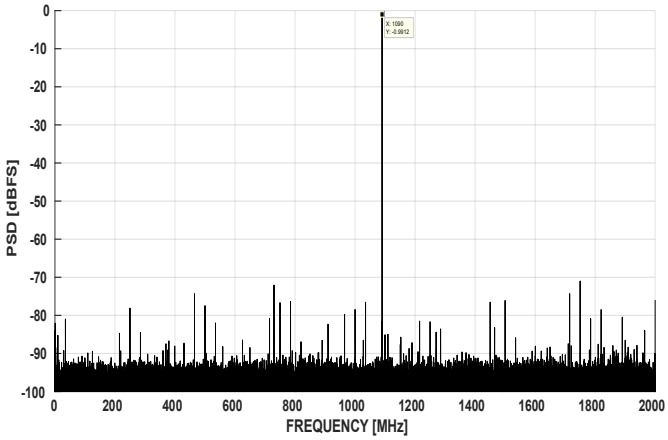


Fig 7-6. FFT at Fin = 1.09GHz, 4GSPS (0.8Vpp FS)

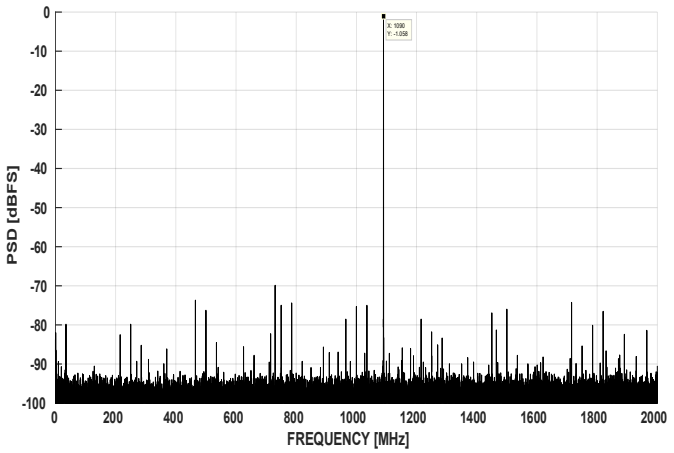


Fig 7-7. FFT at Fin = 1.09GHz, 4GSPS (1.0Vpp FS)

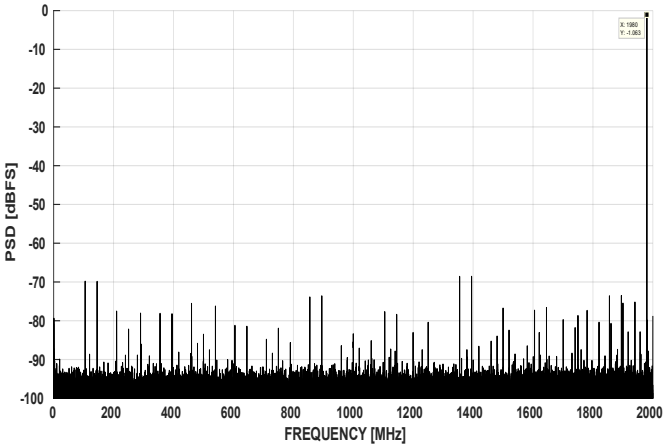


Fig 7-8. FFT at Fin = 1.98GHz, 4GSPS (1.0Vpp FS)

CAE2600
(Single Channel Mode)

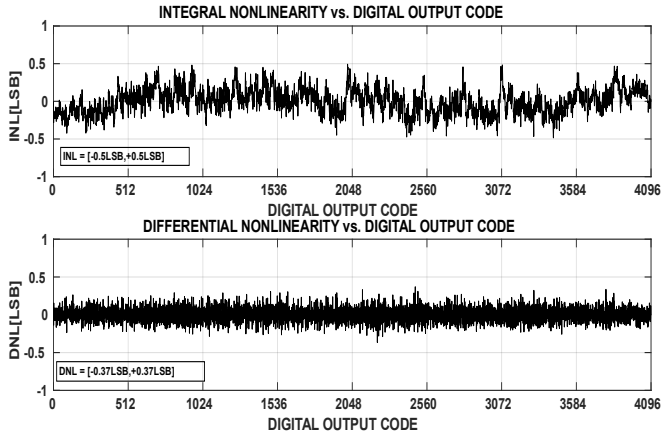


Fig 7-9. INL/DNL at Fin = 110MHz, 2GSPS (1Vpp FS)

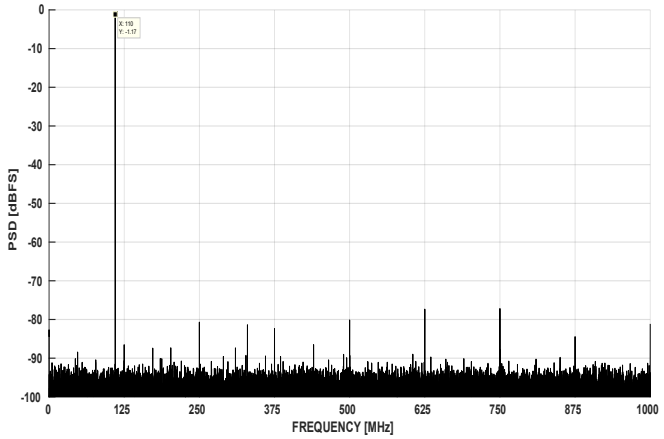


Fig 7-10. FFT at Fin = 110MHz, 2GSPS (1Vpp FS)

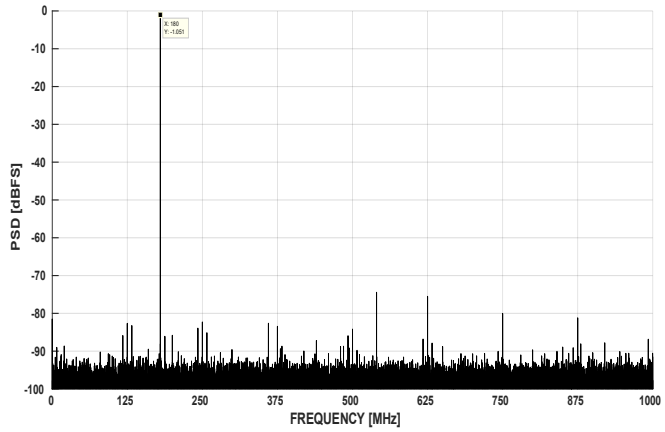


Fig 7-11. FFT at Fin = 180MHz, 2GSPS (1Vpp FS)

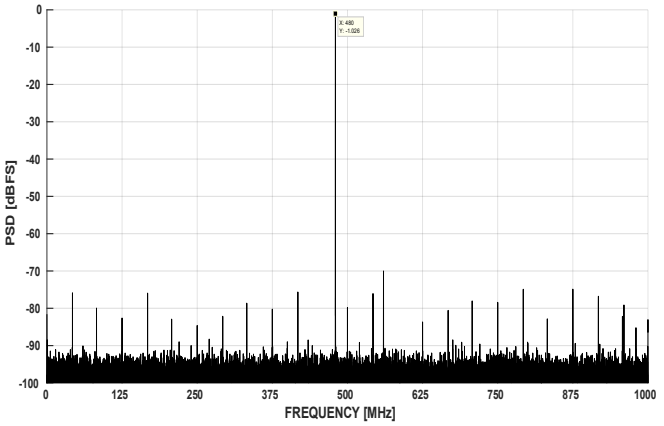


Fig 7-12. FFT at Fin = 480MHz, 2GSPS (1Vpp FS)

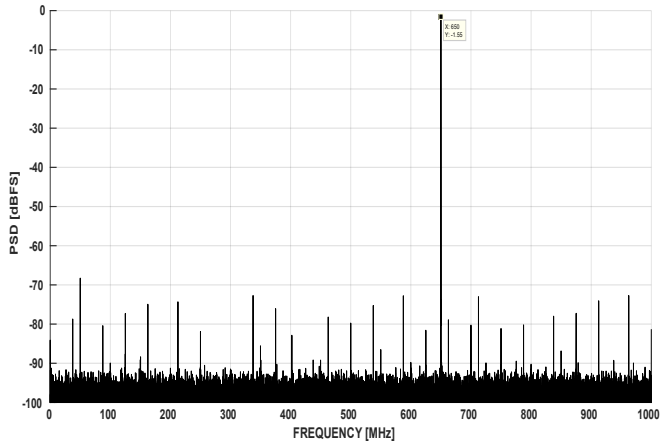


Fig 7-13. FFT at Fin = 600MHz, 2GSPS (1Vpp FS)

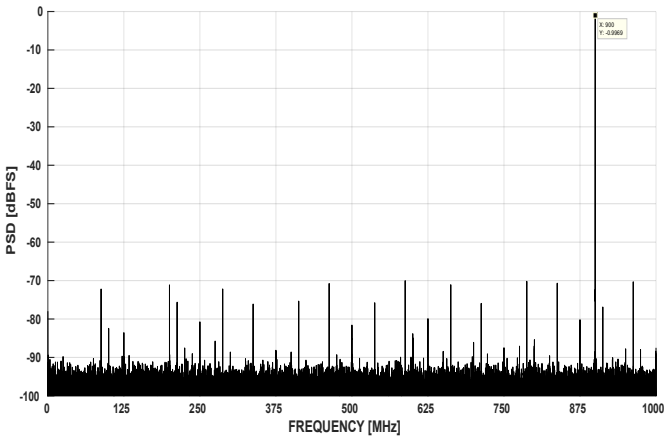


Fig 7-14. FFT at Fin = 900MHz, 2GSPS (1Vpp FS)

CAE2700
(Single Channel Mode)

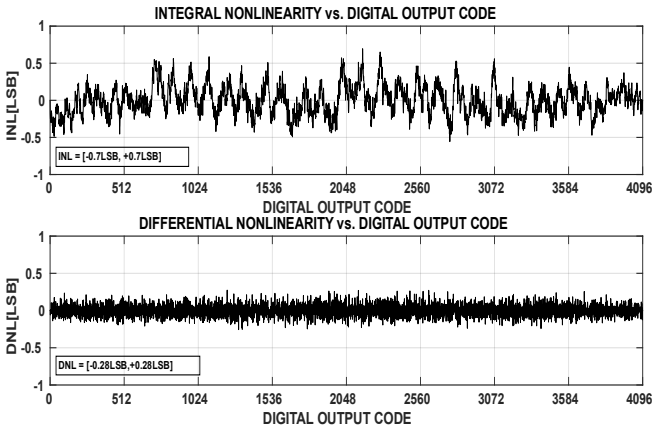


Fig 7-15. INL/DNL at Fin = 110MHz, 1GSPS (1Vpp FS)

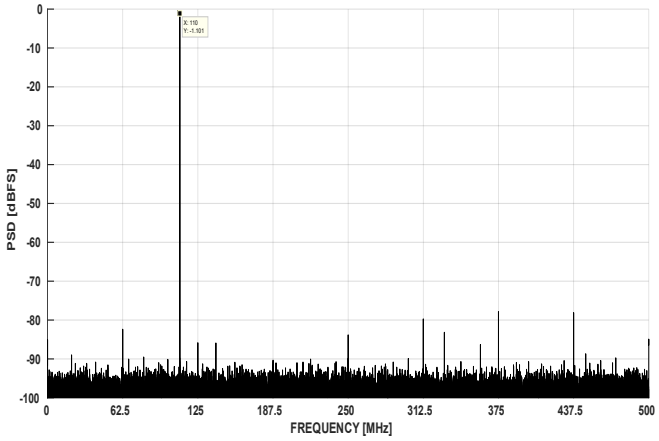


Fig 7-16. FFT at Fin = 110MHz, 1GSPS (1Vpp FS)

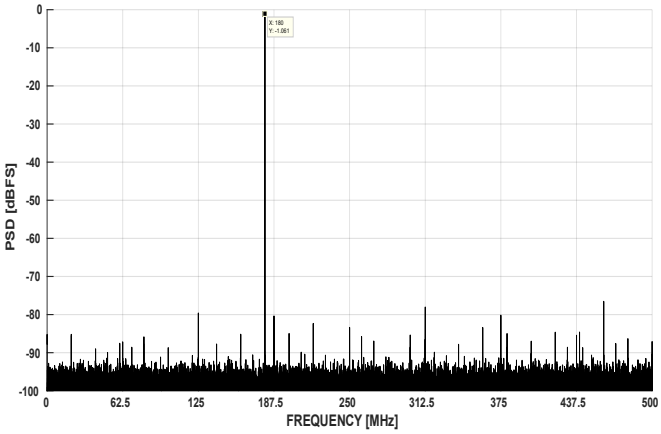


Fig 7-17. FFT at Fin = 180MHz, 1GSPS (1.0Vpp FS)

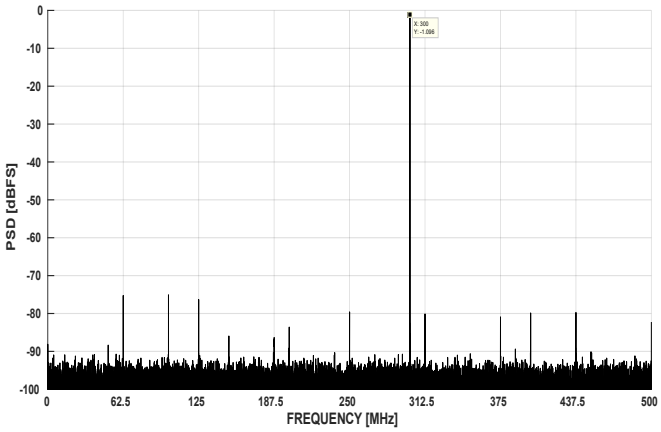


Fig 7-18. FFT at Fin = 300MHz, 1GSPS (1Vpp FS)

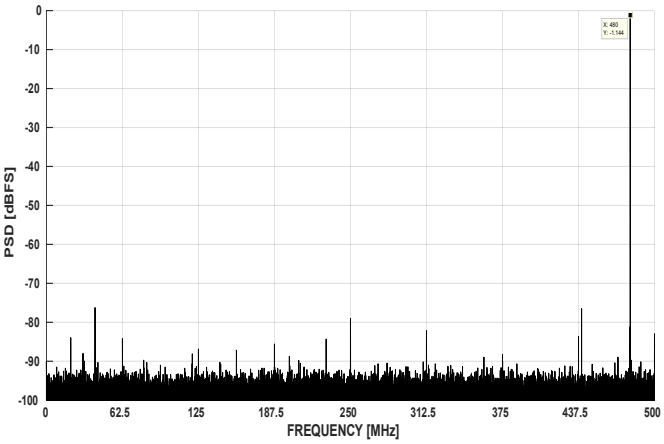


Fig 7-19. FFT at Fin = 400M Hz, 1GSPS (1Vpp FS)

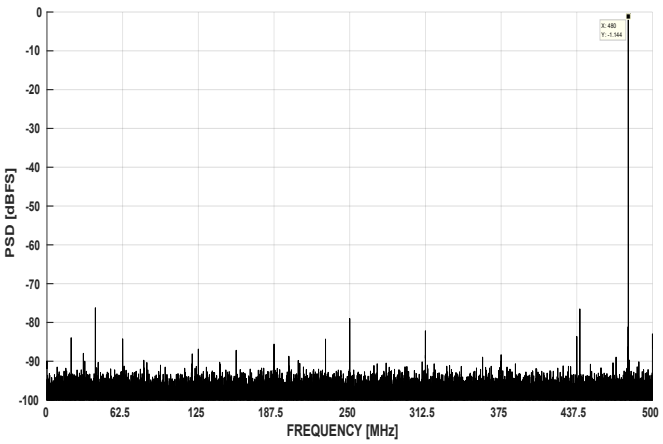


Fig 7-20. FFT at Fin = 480M Hz, 1GSPS (1Vpp FS)

8 Detailed Description

8.1 Overview

CAE2500 is a 12b high speed RF sampling ADC with maximum sampling rate of 4GSPS in single channel mode and maximum sampling rate of 2GSPS in dual channel mode.

CAE2600 is a 12b high speed RF sampling ADC with maximum sampling rate of 2GSPS in single channel mode and maximum sampling rate of 1GSPS in dual channel mode.

CAE2700 is a 12b high speed RF sampling ADC with maximum sampling rate of 1GSPS in single channel mode and maximum sampling rate of 0.5GSPS in dual channel mode.

The chip can be configured as single channel mode or dual channel mode by SPI setting, which supports multiple channels or instantaneous wide bandwidth applications.

CAE2500 / CAE2600 / CAE2700 adopt JESD204B interface, with operating junction temperature of -40 to 115°C and use the package of Flip-Chip BGA 196 pins (12mm x 12mm).

8.2 Functional Block Diagram

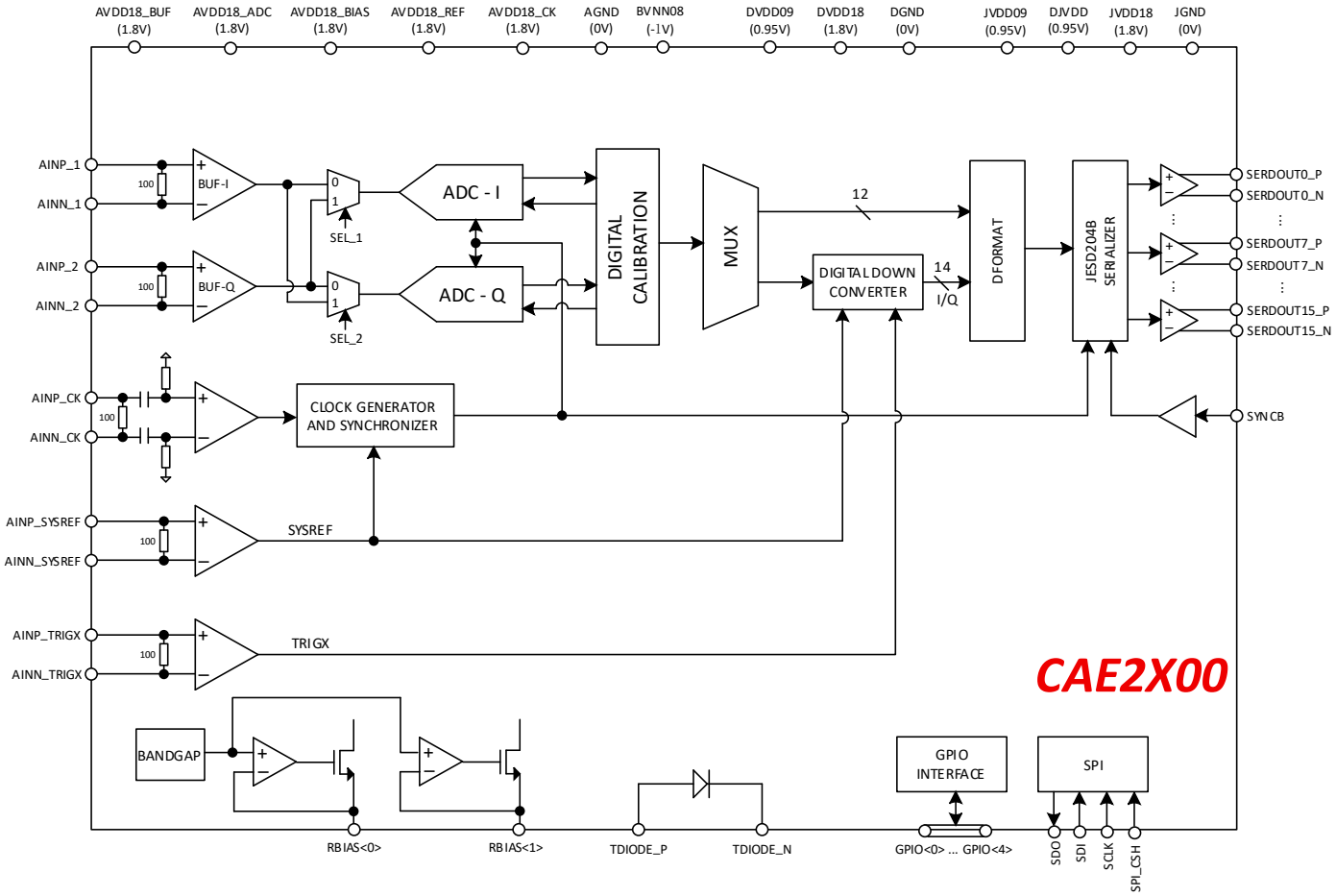


Fig 8-1. Functional Block Diagram

8.3 Signal Pin Connection

CAE2500 / CAE2600 / CAE2700 （For short CAE2X00） all signal pins of the chip can be categorized into 9 groups：

Table 8-1. CAE2X00 Pin Category

Group	Category	# of Pins	Pin Descriptions
1	Analog Input	4	AINP_1 / AINN_1 AINP_2 / AINN_2
2	Main Clock Input	2	AINP_CK / AINN_CK
3	SYSREF Input	2	AINP_SYSREF / AINN_ SYSREF
4	TRIGX Input	2	AINP_TRIGX / AINN_ TRIGX
5	Current Bias Input	2	RBIAS<0> 、 RBIAS<1>
6	Temperature Diode Input	2	TDIODE_P / TDIODE_N
7	Digital I/O Input (1.8V DC level)	13	RESET_ANALOG 、 RESET_LOGIC TSKEW_BG 、 GPIO<0> GPIO<1> 、 GPIO<2> GPIO<3> 、 GPIO<4> SDI 、 SCLK 、 SPI_CSH POWERDOWN 、 SYNCB
8	Digital I/O Output (1.8V DC Level)	3	FD<0> 、 FD<1> 、 SDO
9	JESD204B SerDes Output	32	SERDOUT0_P / SERDOUT0_N SERDOUT1_P / SERDOUT1_N SERDOUT2_P / SERDOUT2_N SERDOUT3_P / SERDOUT3_N SERDOUT4_P / SERDOUT4_N SERDOUT5_P / SERDOUT5_N SERDOUT6_P / SERDOUT6_N SERDOUT7_P / SERDOUT7_N SERDOUT8_P / SERDOUT8_N SERDOUT9_P / SERDOUT9_N SERDOUT10_P / SERDOUT10_N SERDOUT11_P / SERDOUT11_N SERDOUT12_P / SERDOUT12_N SERDOUT13_P / SERDOUT13_N SERDOUT14_P / SERDOUT14_N SERDOUT15_P / SERDOUT15_N

8.3.1 Analog Signal Input AINP_1 / AINN_1 、 AINP_2 / AINN_2

The analog differential input is internally connected to a 100-ohm differential resistor with AINP_1 / AINN_1 for I-channel and AINP_2 / AINN_2 for Q-channel when CAE2X00 is in dual mode.

In single mode, either AINP_1 / AINN_1 or AINP_2 / AINN_2 is required to apply input signal to CAE2X00.

There is a clamp diode attached in each differential input to limit signal swing applied to the internal circuitry for burnt out protection.

In PCB design, all analog signal route must follow proper characteristic impedance matching with 50 ohm single-ended and 100-ohm differential. Improper impedance matching may induce signal reflection back to the source or non-uniform gain flatness. And it is suggested that the analog signal route should avoid the use of VIAs in PCB trace routing and should make good isolation to ensure high quality of signal integrity.

To reduce significant insertion loss, either Rogers RO4350B or Panasonic M6 should be chosen as the materials of PCB.

AC-Coupled

As shown in Fig 8.2, it is in the case of AC coupled of analog input differential signal.

The input common mode of analog differential input of CAE2X00 (VCMI) is 0.45V that is generated by a resistive ladder connected to 1.8V analog power supply.

VCMI is applied to each analog pin through a 2k ohm resistor.

Notice that it is better to separate the VCMI of two analog differential inputs in dual mode of CAE2X00.

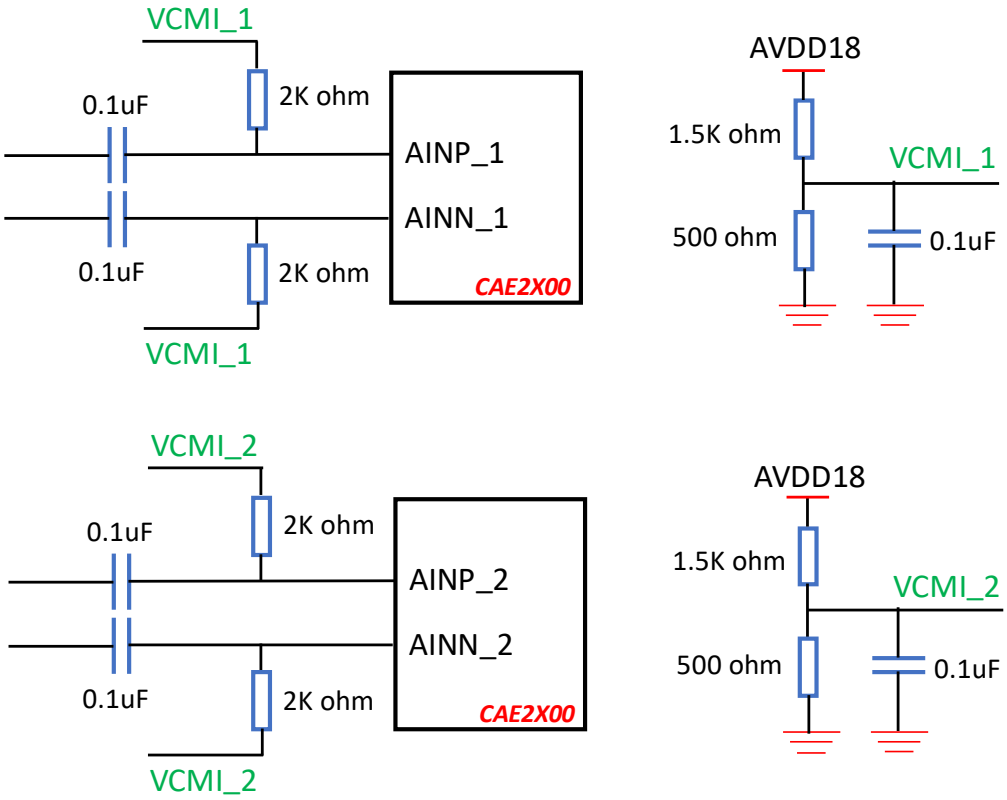


Fig 8-2. AC Coupled Configuration of Analog Input Connection Diagram

DC Coupled

As shown in Fig. 8-3, for DC coupled, the analog differential signal should be driven by the front-end input buffer or wideband amplifier with 0.45V proper common mode provided.

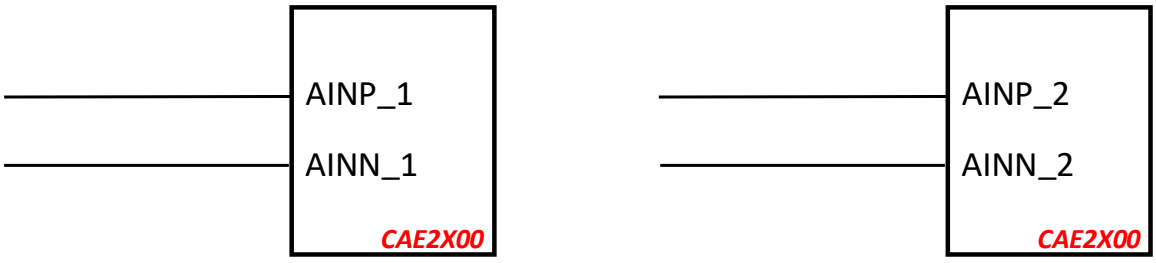


Fig 8-3. DC Coupled Configuration of Analog Input Connection Diagram

8.3.2 Main Clock Input AINP_CK / AINN_CK

For Main Clock input **AINP_CK** / **AINN_CK**, it is only allowed to adopt AC coupled configuration.

As shown in Fig. 8-4, the main clock is coupled to CAE2X00 through 0.1uF capacitor.

To maximize the clock signal swing applied to CAE2X00, a proper VCM_CLK is required to define by a resistive ladder powered by the same power supply of PLL that generates the main clock.

In our example, a 3.3V is used to generate a rough 0.35V VCM_CLK applied to CAE2X00 via a 2K-ohm resistor or higher.

AINP_CK / **AINN_CK** is internally connected to 100-ohm differential resistor with a properly internal defined common mode for on chip clock generator circuitry.

In PCB design, all clock signal route must follow proper characteristic impedance matching with 50 ohm single-ended and 100-ohm differential. Improper impedance matching may induce signal reflection back to the source or poor S11.

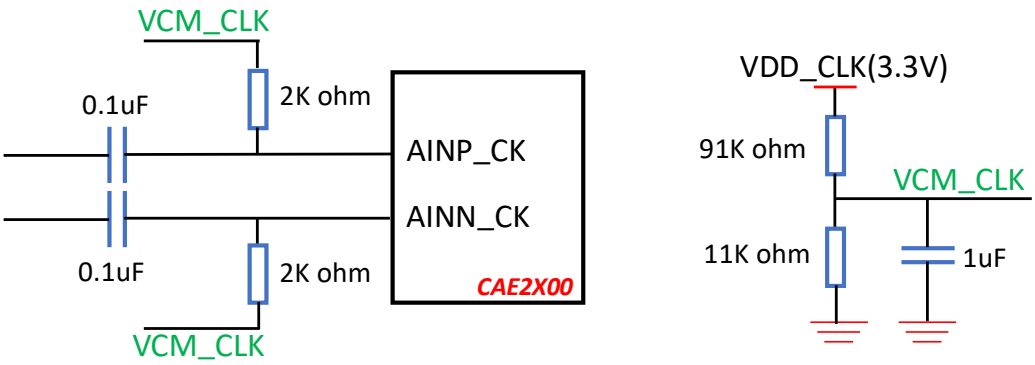


Fig 8-4. Main Clock Input with AC-Coupled Connection Diagram

8.3.3 *SYSREF Input AINP_SYSREF / AINN_ SYSREF*

SYSREF signal allows either DC coupled or AC coupled.

AINP_SYSREF / **AINN_SYSREF** has an internal 100-ohm differential impedance with proper defined common mode internally. In this case, it is not required to define external common mode for these pins in PCB.

In PCB design, all clock signal route must follow proper characteristic impedance matching with 50 ohm single-ended and 100-ohm differential. Improper impedance matching may induce signal reflection back to the source or poor S11.

SYSREF signal is normally generated by PLL with the ability to produce both clock and SYSREF signal.

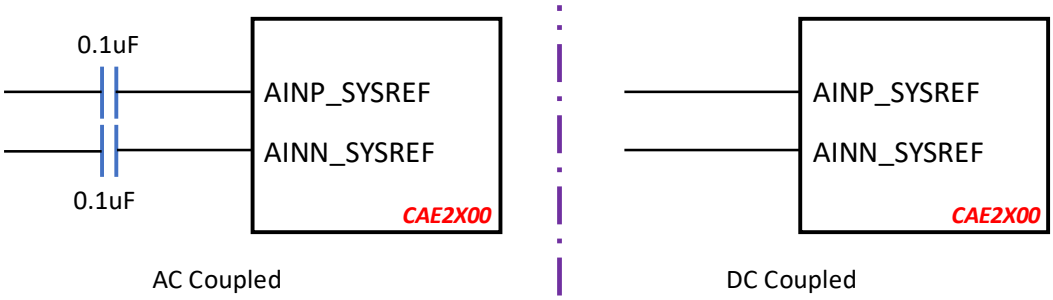


Fig 8-5. SYSREF Input with AC and DC Coupled Connection Diagram

8.3.4 *TRIGX Input AINP_TRIGX / AINN_ TRIGX*

TRIGX signal allows either DC coupled or AC coupled.

AINP_TRIGX / **AINN_ TRIGX** has an internal 100-ohm differential impedance with proper defined common mode internally. In this case, it is not required to define external common mode for these pins in PCB.

In PCB design, all clock signal route must follow proper characteristic impedance matching with 50 ohm single-ended and 100-ohm differential. Improper impedance matching may induce signal reflection back to the source or poor S11.

Differential TRIGX signal is normally generated by FPGA by I/O.

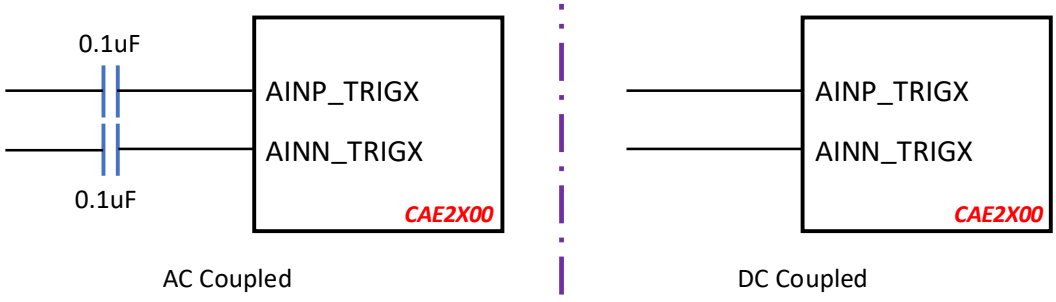


Fig 8-6. TRIGX Input with AC and DC Coupled Connection Diagram

8.3.5 *Analog Current Bias RBIAS<0> 、 RBIAS<1>*

RBIAS<0> 、 RBIAS<1> are used to generate accurate internal reference current.

As shown in Fig. 8-7, they are connected to ground through a 12k ohm resistor with 1% or below accuracy and Tempco of 25ppm/°C or below.

It is suggested to use 0.1% accuracy for more precise current bias.

The 12k ohm resistor is recommended to use 0201 or 0402 package, which is placed to CAE2X00 as closer as possible with good isolation on PCB routing to reduce crosstalk or interference.

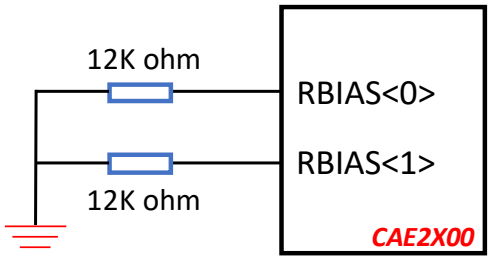


Fig 8-7. Analog Current Bias RBIAS<0> 、 RBIAS<1> Connection Diagram

8.3.6 *Temperature Diode TDIODE_P / TDIODE_N*

TDIODE_P / TDIODE_N is connected to an internal temperature sensed diode inside CAE2X00.

As shown in Fig. 8-8, they are connected to external temperature sensor through a differential lowpass filter formed by R_S and C_{DIFF} to capture the change of DC voltage around TDIODE_P and TDIODE_N due to the change of internal junction temperature.

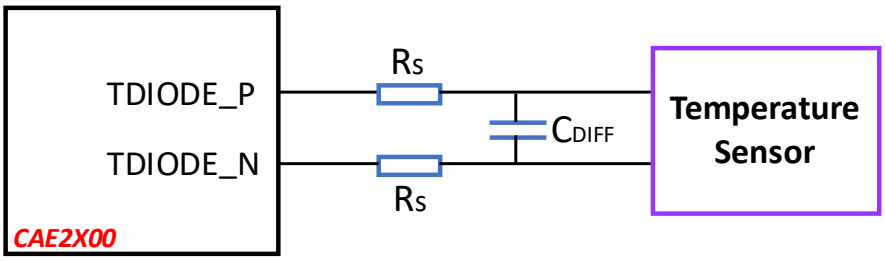


Fig 8-8. Temperature Diode TDIODE_P/TDIODE_N Connection Diagram

8.3.7 *Digital Input I/O (1.8V DC level) RESET_ANALOG 、 RESET_LOGIC 、 TSKEW_BG 、 GPIO<0> 、 GPIO<1> 、 GPIO<2> 、 GPIO<3> 、 GPIO<4> 、 SDI 、 SCLK 、 SPI_CSH 、 POWERDOWN 、 SYNCB*

There is total 13 digital I/O input pins in CAE2X00, the function of each pin can be referred to Table 6.1.

The 5 GPIO pins can only support input I/O but not output I/O.

In Fig. 8-9, the usual connection for all digital I/O is passing through each 0-ohm resistor from I/O of FPGA directly if I/O supply of FPGA is 1.8V.

If it is not 1.8V level, it is required to use each level shifter connected from I/O of FPGA to I/O of CAE2X00 to convert into 1.8V level.

As shown in Fig. 8-9, the external hard reset for “RESET_ANALOG” and “RESET_LOGIC” can also be designed by pressing reset button to pull high the signal level if they are in reset or release button for normal operation.

Notice that all the unused digital I/O pins should be either connected to ground or to I/O supply.

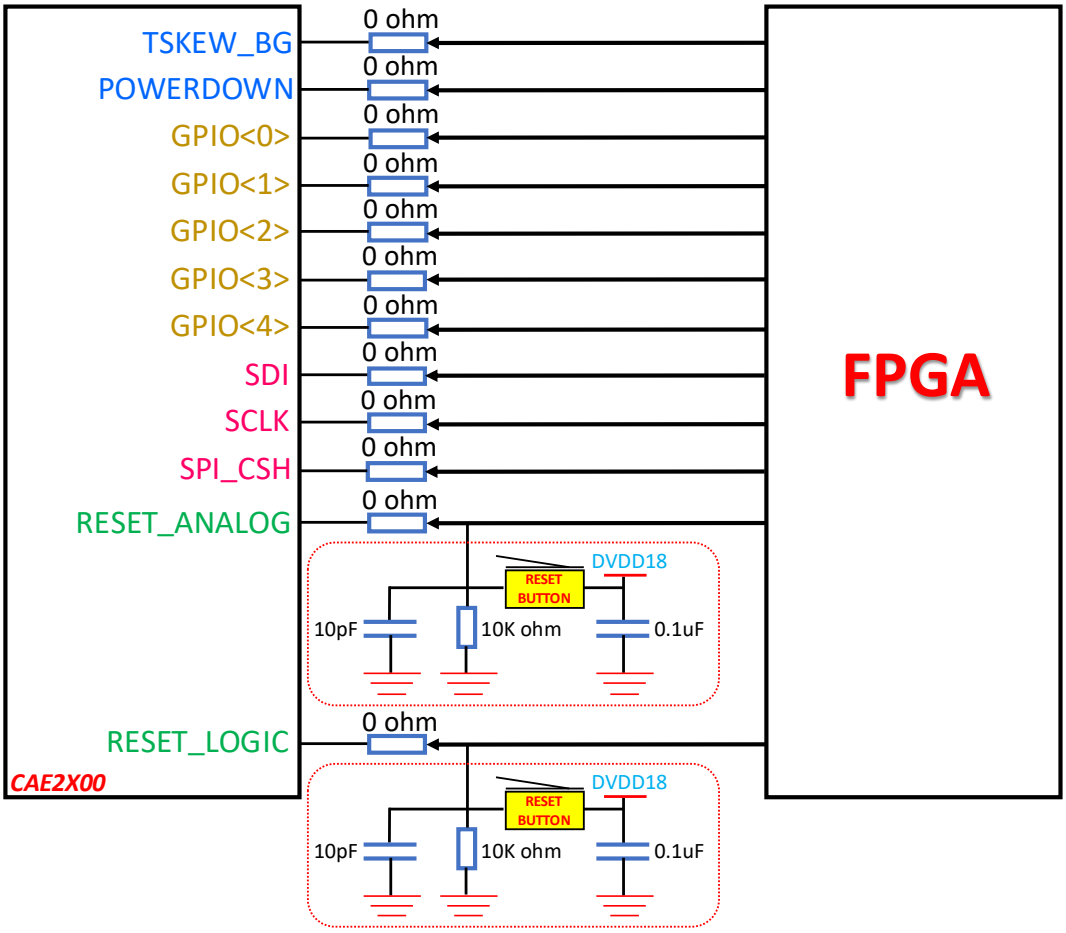


Fig 8-9. Digital Input I/O（1.8V level）Connection Diagram

8.3.8 *Digital Output I/O（1.8V DC level）FD<0>、FD<1>、SDO*

There is total 3 digital output I/O pins in CAE2X00, the function of each pin can be referred to Table 6.1.

In Fig. 8-10, the usual connection for all digital output I/O is passing through each 0-ohm resistor to I/O of FPGA directly if I/O supply of FPGA is 1.8V.

If it is not 1.8V level, it is required to use each level shifter connected from I/O of FPGA to I/O of CAE2X00 to convert into 1.8V level.

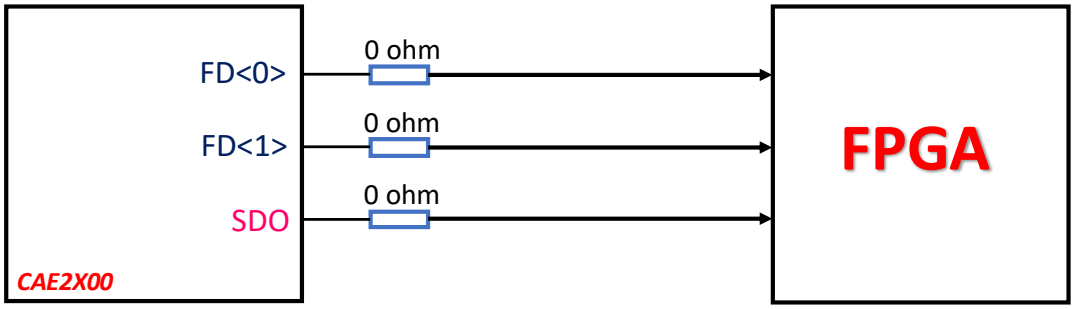


Fig 8-10. Digital Output I/O（1.8V level）Connection Diagram

8.3.9 *JESD204B SerDes Lane Outputs*

SERDOUT0_P / SERDOUT0_N、SERDOUT1_P / SERDOUT1_N、SERDOUT2_P / SERDOUT2_N
SERDOUT3_P / SERDOUT3_N、SERDOUT4_P / SERDOUT4_N、SERDOUT5_P / SERDOUT5_N
SERDOUT6_P / SERDOUT6_N、SERDOUT7_P / SERDOUT7_N、SERDOUT8_P / SERDOUT8_N
SERDOUT9_P / SERDOUT9_N、SERDOUT10_P / SERDOUT10_N、SERDOUT11_P / SERDOUT11_N

SERDOUT12_P / SERDOUT12_N 、SERDOUT13_P / SERDOUT13_N 、SERDOUT14_P / SERDOUT14_N SERDOUT15_P / SERDOUT15_N

There is total 16 differential SerDes lanes output in CAE2X00.

As shown in Fig. 8-11, each lane is connected to RX of JESD204B of FPGA via 0.1uF ac-coupled capacitor.

It is important to route all PCB SerDes lanes strictly following with 50-ohm single-ended or 100-ohm differential impedance matching requirements, make all differential lanes perfectly matched and all lanes have equally length routes.

The crosstalk of SerDes lanes due to adjacent lanes keeps -33dB or below.

To reduce significant insertion loss, either Rogers RO4350B or Panasonic M6 should be chosen as the materials of PCB.

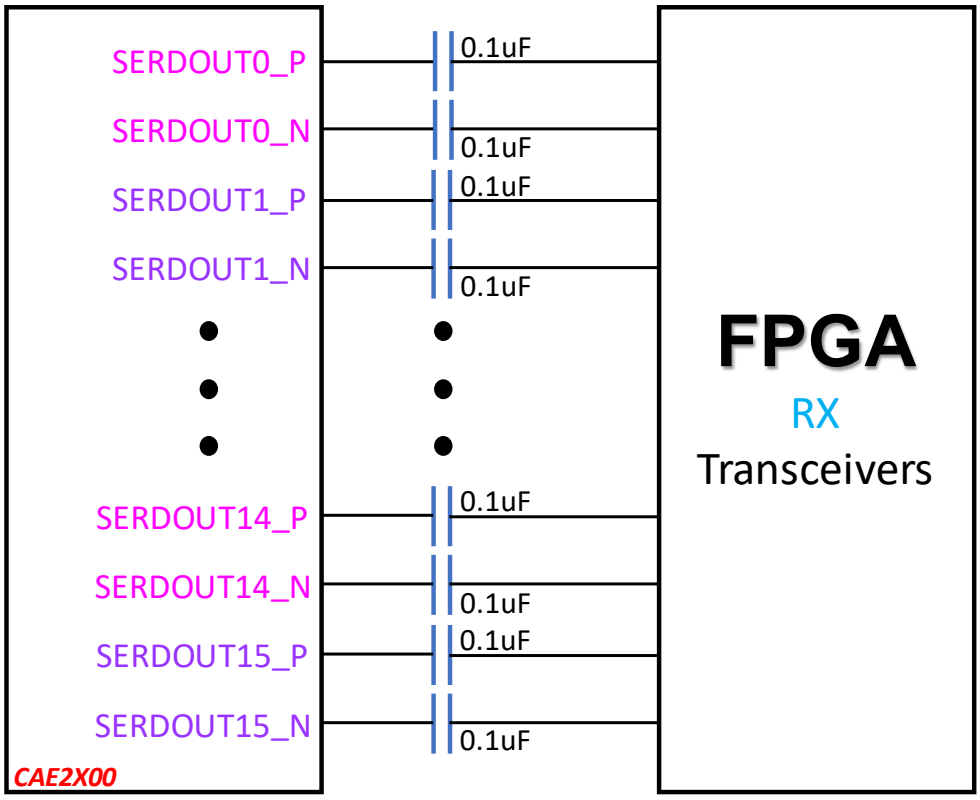


Fig 8-11. JESD204B SerDes Lanes Connection Diagram

8.4 Power Supply

CAE2500 / CAE2600 / CAE2700 (For short **CAE2X00**) 12 groups in 1.8V power supply, 3 groups in 0.95V power supply, 2 groups in -1V power supply.

Fig. 8-12 shows all separated power supply connection diagram of **CAE2X00**. The regulated 12V DC supply is powered by two positive supplies DC/DC converters and one negative supply DC/DC converter. Three DC/DC converters are later powered to four low dropout regulators (LDO) before powering **CAE2X00**.

LDO 1 powered the five analog power supplies (**AVDD18_BUF**, **AVDD18_ADC**, **AVDD18_REF**, **AVDD18_BIAS, AVDD18_CK**) of **CAE2X00** separately via independent Ferrite Beads or Feed Through Filters to reduce or filter out the crosstalk among all five power supplies shared together with the same LDO 1.

LDO 2 powered both digital I/O and JESD204B I/O supplies (**DVDD18, JVDD18**) of **CAE2X00** separately via independent Ferrite Beads or Feed Through Filters to reduce or filter out the crosstalk among two power supplies shared together with the same LDO 2.

LDO 3 powered three core digital, and two core JESD204B supplies (**DVDD09, DJVDD, JVDD09**) of **CAE2X00** separately via independent Ferrite Beads or Feed Through Filters to reduce or filter out the crosstalk among two power supplies shared together with the same LDO 3. If **CAE2X00** doesn't need to use DDC function, maximum current of **DVDD09** is around 800mA.

Both **BVNN08<0>** and **BVNN08<1>** share the same negative LDO 4 in our example if maximum dc current sink by **BVNN08<0>** and **BVNN08<1>** is less than 500mA. If the total current is higher than 500mA, separate negative LDO is required to power the supply of **BVNN08<0>** and **BVNN08<1>** of **CAE2X00**.

The current ratings shown in Fig. 8-12 are the recommended maximum values but the actual values. It is recommended to keep very low parasitic resistance to every power supply and leave enough margin on maximum current ratings. A large power plane allows both lowest parasitic resistance and good heat sink capability.

For power supplies wake up, all 1.8V power supplies should be waked up before 0.95V/-1V power supplies.

Three circuit grounds such as **AGND**, **DGND** and **JGND** are shorted together to the same ground plane in PCB.

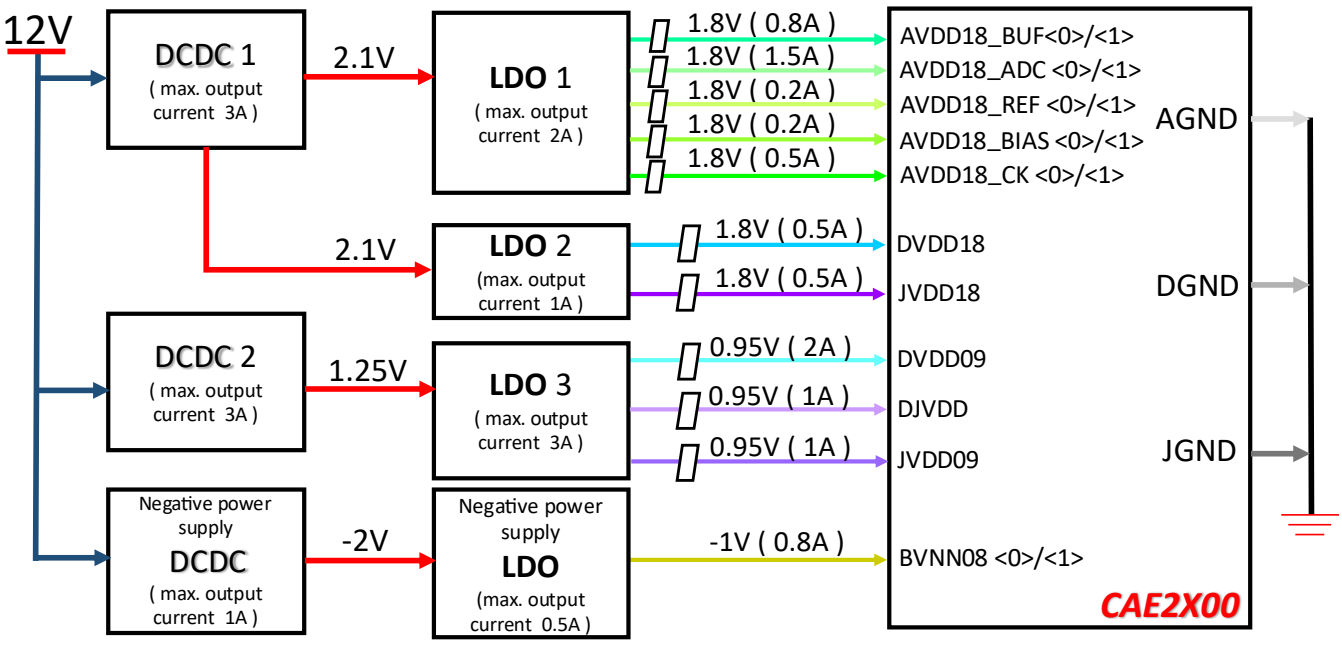


Fig 8-12. CAE2X00 Recommended Isolated Power Supply Connection Diagram

(In Fig. 8-12, the supply voltages shown in DC/DC or LDO are an example of our EVM. Users should adjust appropriate supply voltages according to the actual DC/DC and LDO used in their design)

Fig. 8-13 shows the combined power supply connections of **CAE2X00**.

The four 1.8V analog power supplies (**AVDD18_BUF**、**AVDD18_ADC**、**AVDD18_REF**、**AVDD18_BIAS**) share the same 1.8V supply source whereas **AVDD18_CK** connects a separate 1.8V supply source. Two 1.8V supply sources are connected to LDO 1 via independent Ferrite Beads or Feed Through Filters.

The two 0.95V core JESD204B supplies (**DJVDD** and **JVDD09**) share the same 0.95V supply source whereas **DVDD09** connects a separate 0.95V supply source. Two 0.95V supply sources are connected to LDO 3 via independent Ferrite Beads or Feed Through Filters.

The current ratings shown in Fig. 8-13 are the recommended maximum values but the actual values. It is recommended to keep very low parasitic resistance to every power supply and leave enough margin on maximum current ratings. A large power plane allows both lowest parasitic resistance and good heat sink capability.

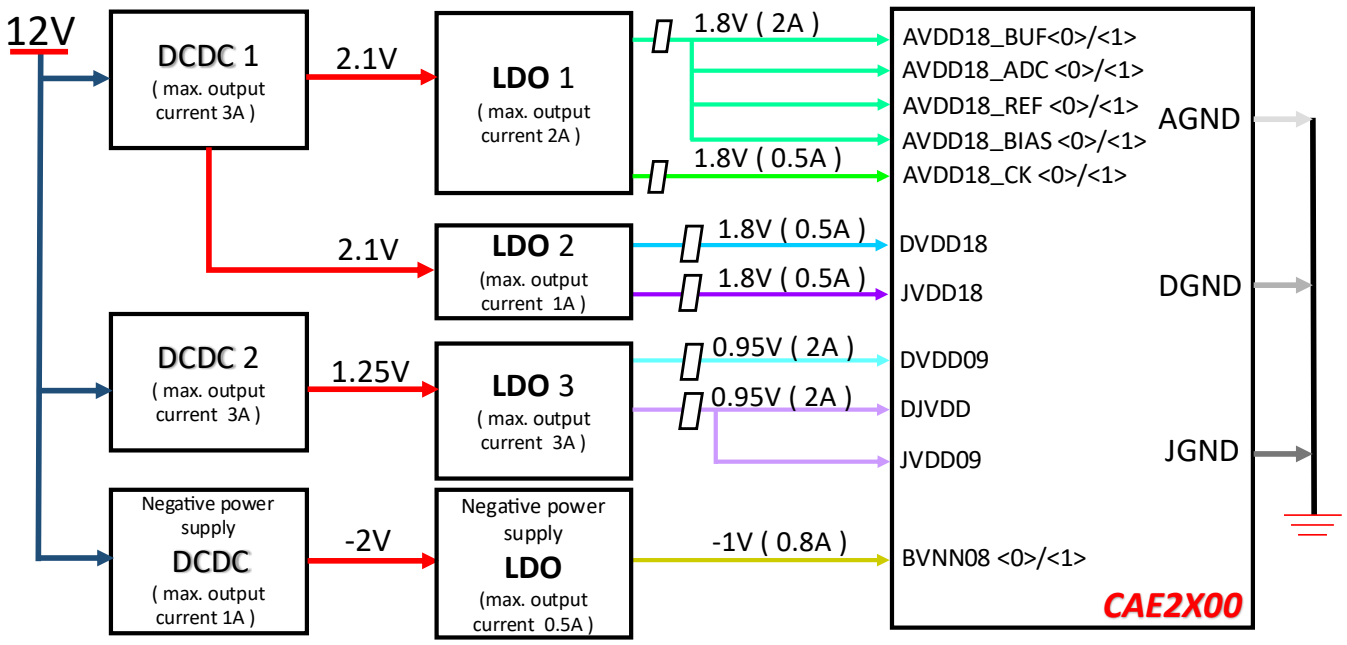


Fig 8-13. CAE2X00 Recommended Combined Power Supply Connection Diagram

8.5 Decoupling Capacitor on Power Supply

Figure 8-14 is a reference diagram showing the placement of filter capacitors near the power pins of the **CAE2X00**. The diagram assumes the PCB uses a resin-filled via process and the filter capacitor package size is 0201. In this case, the filter capacitor can be placed on the back of the PCB at the power pin and GND pin positions of the **CAE2X00**.

It is important to note that the capacitors at the NC pin and DJVDD pin positions in the diagram only indicate that a 0201 package filter capacitor can be placed at these positions when the NC pin is floating and there are no vias on the pad, and the actual ground plane below the NC pin on the back of the PCB is GND. Grounding the NC pin or connecting the NC pin to the DJVDD power pin with a capacitor may cause the ADC chip to malfunction.

The AVDD18 capacitor position in the diagram represents a recommended reserved capacitor pad on the PCB. The actual number of surface-mount capacitors can be adjusted based on the specific power supply and routing configuration. If all capacitor positions are not surface-mounted, the surface-mount capacitors should be placed as evenly and staggered as possible, avoiding placing capacitors only on one side or a few power pins.

For **DVDD18** and **JVDD18** power supplies, it is recommended to add one or two capacitor slots near the ADC chip.

For filter capacitors, it is recommended to use a combination of one 1uF capacitor and multiple 0.1uF capacitors to reduce low-frequency and high-frequency noise in the power supply.

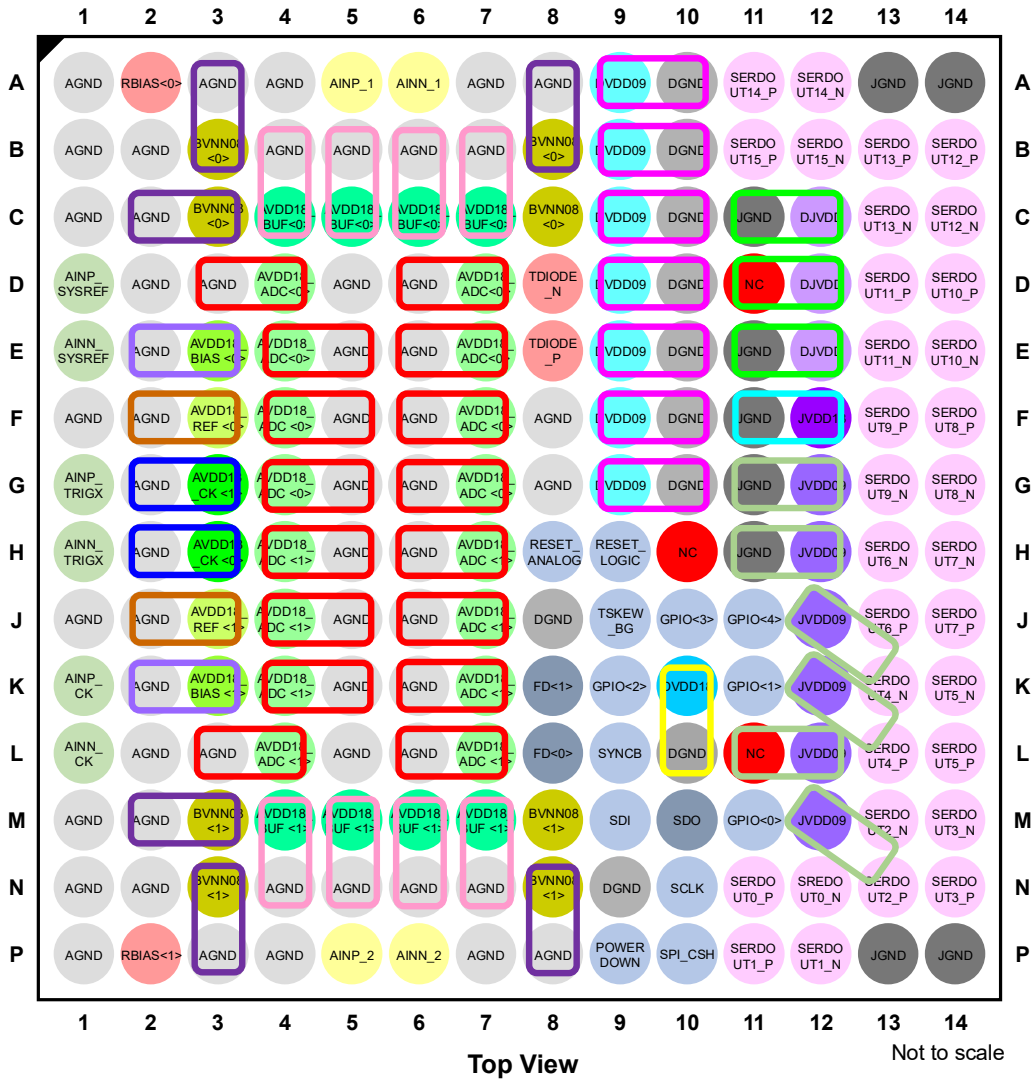


Fig 8-14. Recommend Decoupling Capacitor Placement on Power Supplies

9 Memory Map

In CAE2X00, registers are divided into two categories such as SPI control registers and JESD204B registers.

9.1 SPI Control Registers

Table 9-1. SPI Control Register List

No.	Register Name	Register Address	Default Value
1	Timing Skew Control Register	9h05	32'h0042_9648
2	Output Mode Control Register	9h06	32'h4000_7958
3	Aperture Delay Register	9h89	
4	FD Dwell Register	9h15F	32'h0000_0000
5	FS Range Control Register	9h15D	32'h0000_9B9B
6	Fast Threshold Detection Register	9h15E	32'h0000_0000
7	Analog Input Channel Register	9h02	32'h8003_8FFF
8	DDC PST Control Register	9h1C	32'h0010_0000
9	DDC NCO Control Register	9h07	32'h0301_0000
10	DDC PHASE Control Register		
11	DDC FTW Control Register		
12	DDC Control Register	9h01	32'h8000_4000

Timing Skew Control Register (Address 9h05 32'h0042_9648)

Bits	Name	Default	Descriptions
31	bg_always	1'b0	Background timing skew always do 1 : enable 0 : disable
30	bg_fpga	1'b0	FPGA background timing skew enable 1 : enable 0 : disable
29	tskew_hd_en	1'b0	Tskew_bg_pin enables control background timing skew 1 : enable 0 : disable
28:27	Uf_range	2'h00	Ultra_fine ok range : 00 : 1 01 : 2 10 : 3 11 : 4
26:24	bgpd_mode	3'h000	Background timing skew power down timing set 000 : 50ms 001 : 100ms 010 : 200ms 011 : 300ms 100 : 700ms 101 : 1500ms 110 : 3100ms 111 : 6300ms
23	Ufwin_en	1'b0	Ultra_Fine_detect window function (check ultra fine cap margin of stable) enable 1 : enable 0 : disable
22:20	tsrx_th	3'b100	Timing skew matrix result/N 000 : 1 001 : div2 010 : div4 011 : div8 100 : div16
19	tsfir_en	1'b0	1 : Timing skew input FIR enable 0 : disable (default)
18	Dual_mode	1'b0	1 : dual channel mode 0 : single channel mode(default)
17	fg_mode_spi	1'b1	Force Fine Cap MSB result=1 1 : enable 0 : disable

Timing Skew Control Register (Address 9h05 32'h0042_9648) (Cont'd)

Bits	Name	Default	Descriptions
16	sel_otp_data	1'b0	1 : Timing skew mode1/2 start from efuse value 0 : Timing skew mode1/2 start from current value
15:14	bg_thres	2'b10	Background timing skew result overflow threshold Lower threshold upper threshold 00 : 0 63 01 : 4 59 10 : 8 55 01 : 16 47
13:12	bg_mode	2'b01	background timing skew mode 00 : Used in factory test mode or Reset all 7b coarse, 6b fine and 6b ultra-fine codes mode 01 : Used in user mode (most often case): Keep the current 6b coarse and 6b fine codes, while loop [+1,0, -1] LSB on 6b ultrafine. This cases is looping programmable [8,16,32,64,128,256,512,1024] times, if it is still out of range or divergence, it goes to "10" mode 10 : Keep the current 6b coarse and 6b fine codes, reset all 6b ultra-fine code, first loop [+1,0, -1] LSB on 6b fine delay code and then loop [+1,0,-1] LSB on 6b ultra-fine delay code. If 6b fine after looping, it is out of range or divergence. It goes to "11" mode. Otherwise, if 6b fine is within pre-set range, only ultra-fine 6b codes are out of range. It goes to "01" mode. If both 6b fine codes and 6b ultra-fine codes are within pre-set range, it terminates the calibration. 11 : Reset all 6b fine and 6b ultra-fine codes mode, looping 7b coarse code. If 7b coarse codes are within pre-set range, it goes to loop 6b fine and then 6b ultra-fine. If 7b coarse codes are out of range, it goes to "00" mode.
11:8	tskew_mode	4'b0110	Timing skew discard/average samples setting 0000 : discard/average number 2^17 0001 : discard/average number 2^18 0010 : discard/average number 2^19 0011 : discard/average number 2^20 0100 : discard/average number 2^21 0101 : discard/average number 2^22 0110 : discard/average number 2^23 0111 : discard/average number 2^24 1000 : discard/average number 2^25 1001 : discard/average number 2^26 1010 : discard/average number 2^27 1011 : discard/average number 2^28 1100 : discard/average number 2^29 1101 : discard/average number 2^30 1110 : discard/average number 2^31 1111 : discard/average number 2^32
7	inv_ts_mode	1'b0	Timing skew sgn result inverse 1 : enable 0 : disable
6:4	bg_ts_mode	3'b100	Background timing skew loop number 000 : 32loop 001 : 64loop 101 : 128loop 110 : 256loop 111 : 512loop
3:2	bg_repeat	2'b10	Decision loop number for majority result: Identical Trials Success Threshold 00 : 1 1 01 : 4 3 10 : 8 6 11 : 16 12
1	tskew_bg	1'b0	Background timing skew enable 1 : enable 0 : disable
0	RVD		

Output Mode Control Register (Address 9h06 32'h4000_7958)

Bits	Name	Default	Descriptions
31:8	RVD		
7	p2SnOf	1'b1	1 : output 2's code 0 : output offset code
6:0	RVD		

Aperture Delay Register (Address 9h89)

Bits	Name	Default	Descriptions
31:23	aper_delay[8:0]	9'd0	Noiseless aperture delay (tAD) adjustment, average 5ps/step
22:0	RVD		

FD Dwell Register (Address 9h15F 32'h0000_0000)

Bits	Name	Default	Descriptions
31:16	Fd_dwell_4B	16'h0	Sar4B dwell time counter target. The fast detect goes low if the analog input is below the fast detect lower threshold value for greater than this 16bits programmable data clock (fs/16 or dual mode fs/8) counter.
15:0	Fd_dwell	16'h0	Sar12b dwell time counter target. The fast detect goes low if the analog input is below the fast detect lower threshold value for greater than this 16bits programmable data clock (fs/16 or dual mode fs/8) counter.

FS Range Control Register (Address 9h15D 32'h0000_9B9B)

Bits	Name	Default	Descriptions
31:16	RVD		
15:8	Fs_range_B	8'h9B	AINP_2/AINN_2 full scale voltage adjust: 2mv/step, from 0.5V-1V FS_RANGE_B = FS_RANGE_A if single channel mode.
7:0	Fs_range_A	8'h9B	AINP_1/AINN_1 full scale voltage adjust: 2mv/step, from 0.5V-1V

Fast Threshold Detection Register (Address 9h15E 32'h0000_0000)

Bits	Name	Default	Descriptions
31	RVD		
30:28	Fd4b_up	3'h0	Sar4B upper threshold. 4-bit value for the fast detect upper threshold. The fast detect goes high if the analog input(offset code high 4B) is above or equal with the upper threshold value for one data clock (fs/16 or dual mode fs/8) cycle. Fd4b_up sar4B offset code 000 1111 001 1110 010 1101 011 1100 100 1011 101 1010 110 1001 111 1000
26:16	Fd_up	11'h0	12B upper threshold. 11-bit value for the fast detect upper threshold. The fast detect goes high if the analog input (2s complement code abs value) is above the upper threshold value for one data clock (fs/16 or dual mode fs/8) cycle.
15:13	Fd4b_lo	3'h0	Sar4B lower threshold unsigned number. 4-bit value for the fast detect lower threshold. The fast detection goes low if the analog input (offset code high 4B) is below the lower threshold value for FD_dwell_4B time.
12	P4Bn12	1'b0	1 : sar4B mode 0 : 12b output data mode
11	fden	1'b0	Fast threshold detection enable 1 : enable 0 : disable
10:0	Fd_low	11'h0	Sar12B mode lower threshold unsigned number. 11-bit value for the fast detect lower threshold. The fast detect goes low if the analog input(2s complement code abs value) is below the lower threshold value for FD_dwell time.

Analog Input Channel Register (Address 9h02 32'h8003_8FFF)

Bits	Name	Default	Descriptions
31:21	RVD		
20	SEL_BUF_CH	1'b0	analog buffer input setting for single channel mode 1 : Q_channel (AINP_2 / AINN_2) 0 : I_channel (AINP_1 / AINN_1)
19:0	RVD		

DDC PST Control Register (Address 9h1C 32'h0010_0000)

Bits	Name	Default	Descriptions
31:0	PST	32'h0010_0000	profile timer number

DDC NCO Control Register (Address 9h07 32'h0301_0000)

Bits	Name	Default	Descriptions
31:27	RVD		
26:24	sync_en, sync_next, trig_rst_en	3'b011	Register setting description SYSREF_x edge used to synchronize the PAWs 100 : all subsequent edges for SYSREF_x signal reset all the PAWs in the chip 110 : the next valid edge of SYSREF_x signal reset all the PAWs in the chip 001 : all edges of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip 011 : the next valid edge of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip
23:20	nco_nu_mode	4'h0000	NCO number mode. 4'b0000 : NCO from reg 4'b10xx : NCO from edge 4'b01xx : NCO from GPIO 4'b1100 : NCO from profile select timer
19:18	reg_nu	2'b00	NCO number from register : choose one of 4 NCO
17	Trig_spi	1'b0	Implement TRIGX pin function with SPI 1 : enable 0 : disable
16	PD_TRIG	1'b1	1 : power down TRIGX pin 0 : power on and TRIGX pin control enable
15:8	Sysref_delay	8'h00	Programable delay on SYSREF path to DDC NCO, 8-bit delay in terms of data clock (single channel mode fs/16 or dual channel mode fs/8)
7:0	Trig_delay	8'h00	Programable delay on TRIGX path to DDC NCO, 8-bit delay in terms of data clock (single channel mode fs/16 or dual channel mode fs/8)

(Note: nco_nu_mode = 4'b1000, GPIO[0] low to high transition determines the exact nco_number. The first NCO number is 0 , GPIO[0] 0->1 will increment the NCO number by 1. If The NCO number is equal to reg_nu , the next GPIO[0] 0 –> 1 will loop back the NCO number to 0.

nco_nu_mode = 4'b1001, NCO number selected from GPIO[1] 0->1 edge transition;

nco_nu_mode = 4'b1010 , NCO number selected from GPIO[2] 0->1 edge transition;

nco_nu_mode = 4'b1011 , NCO number selected from GPIO[3] 0->1 edge transition ;

nco_nu_mode = 4'b0100 , NCO number selected by GPIO[0] . if GPIO[0]=0 , then NCO number is 0; if GPIO[0]=1 , then NCO number is 1;

nco_nu_mode = 4'b0101, NCO number selected by GPIO[1:0]; GPIO[1:0]=2'd0 NCO number 0; GPIO[1:0]=2'd1 NCO number 1; GPIO[1:0]=2'd2 NCO number 2; GPIO[1:0]=2'd3 NCO number 3;

nco_nu_mode = 4'b1100 , NCO number selected by PST counter. The profile select timer specifies the number of data clock cycles between frequency hops, and the NCO channel increments when the profile select timer expires. The NCO number loop backs to 0 when NCO number is equal to reg_nu and is incremented .(mean 0,1..reg_num,0,1…, and so on)

DDC PHASE Control Register： only 4 NCO support if single channel mode, set phas0—phase3. in dual channel mode, phase4--phase7 for the second analog input channel

Bits	Name	Default	Descriptions
47:0	{reg168[15:0] ,reg160[31:0]}	48'd32056872347602	Phase0: 41 degree (41/360) * 2^48
47:0	{reg168[31:16],reg161[31:0]}	48'd32056872347602	Phase1: 41 degree (41/360) * 2^48
47:0	{reg169[15:0] ,reg162[31:0]}	48'd32056872347602	Phase2:41 degree (41/360) * 2^48
47:0	{reg169[31:16],reg163[31:0]}	48'd32056872347602	Phase3:41 degree (41/360) * 2^48
47:0	{reg16a[15:0] ,reg164[31:0]}	48'd30493122476988	Phase4:39 degree (39/360) * 2^48
47:0	{reg16a[31:16],reg165[31:0]}	48'd30493122476988	Phase5:39 degree (39/360) * 2^48
47:0	{reg16b[15:0] ,reg166[31:0]}	48'd30493122476988	Phase6:39 degree (39/360) * 2^48
47:0	{reg16b[31:16],reg167[31:0]}	48'd30493122476988	Phase7:39 degree (39/360) * 2^48

DDC FTW Control Register： only 4 NCO support if single channel mode, set FTW0--FTW3. in dual channel mode, FTW4--FTW7 for the second analog input channel

Bits	Name	Default	Descriptions
47:0	{reg150[15:0] ,reg16C[31:0]}	48'd136339441844233	FTW0:
47:0	{reg150[31:16],reg16D[31:0]}	48'd32985348833280	FTW1:
47:0	{reg151[15:0] ,reg16E[31:0]}	48'd65970697666560	FTW2:
47:0	{reg151[31:16],reg16F[31:0]}	48'd136339441844233	FTW3:
47:0	{reg156[15:0] ,reg152[31:0]}	48'd136339441844233	FTW4:
47:0	{reg156[31:16],reg153[31:0]}	48'd32985348833280	FTW5:
47:0	{reg157[15:0] ,reg154[31:0]}	48'd67114189759447	FTW6:
47:0	{reg157[31:16],reg155[31:0]}	48'd136339441844233	FTW7:

DDC Control Registers (Address 9h01 32'h8000_4000)

Bits	Name	Default	Descriptions
31	ddc_soft_rstb	1'b1	Write 0 will reset DDC module
30:28	Uf_window	3'h0	Timing skew Ultra_Fine Cap steady window value. 0 : 8 1 : 16 2 : 32 3 : 64 4 : 128 5 : 256 6 : 512 7 : 1024
27:25	Adcen_dt	3'h0	ADC_EN programmable delay time. 0 : 0us 1 : 100us 2 : 300us 3 : 450us 4 : 600us 5 : 800us 6 : 1ms 7 : 1.5ms
24	Mid_tskew	1'b0	1 : Background timing skew mode0 start from middle value1000_0000 0 : current value
23:18	RVD		
17	Ddc_fs4	1'b0	1/4 Fs IF mode 1 : enable 0 : disable
16	ddc_zif	1'b0	NCO Zero IF , no need NCO and mixer 1 : enable 0 : disable
15:13	ddc_mac_mode	3'b100	DDC MA average number. 0 : 2^14, 1 : 2^15 2 : 2^16 3 : 2^17 4 : 2^18 5 : 2^19 6 : 2^20 7 : 2^21
12	ddc_debug_mode	1'b0	1 : DDC result MA from SPI; 0 : from MA module
11	ddc_test_mode	1'b0	The input samples are forced to positive full scale and the NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters
10	ddc_gain_6db	1'b0	1 : DDC gain 6dB 0 : DDC gain 0dB
9	ddc_c2r_en	1'b0	DDC Complex to real enable 1 : enable 0 : disable
8	hb1_en	1'b0	DDC Hb1 FIR enable 1 : enable 0 : disable
7	tb2_en	1'b0	DDC Tb2 FIR enable 1 : enable 0 : disable
6	hb2_en	1'b0	DDC Hb2 FIR enable 1 : enable 0 : disable
5	hb3_en	1'b0	DDC Hb3 FIR enable 1 : enable 0 : disable
4	hb4_en	1'b0	DDC Hb4 FIR enable 1 : enable 0 : disable
3	hb5_en	1'b0	DDC Hb5 FIR enable 1 : enable 0 : disable
2	hb6_en	1'b0	DDC Hb6 FIR enable 1 : enable 0 : disable
1	hb7_en	1'b0	DDC Hb7 FIR enable 1 : enable 0 : disable
0	ddcen	1'b0	DDC enable 1 : enable 0 : disable

9.2 JESD204B Registers

JESD204B APB Read/Write Register

Begin Address	End Address	Range	module
0x00	0x7F	7bits	JESD204B MAC
0x80	0xFF	7bits	JESD204B PMA PHY

MAC Register

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x000	version_1	[7:0]	version_1		version number 1	0x20	R
0x001	version_2	[7:0]	version_2		version number 2	0x23	R
0x002	version_3	[7:0]	version_3		version number 3	0x05	R
0x003	version_4	[7:0]	version_4		version number 4	0x31	R
0x004	test	[7:0]	test_reg		reg for r/w test.	0x0	R/W
0x005	global_ctrl	[7]	PMA_pwrdn	0 1	204B IP power down control bit normal work power down	0x0	R/W
		[6:0]	Reserved		Reserved.	0x0	R
0x010	Sync mode	[7:3]	Reserved		Reserved.	0x0	R
		[2:1]	SYSREF± mode select	0 1 10	Disabled. Continuous. One-shot.	0x0	R/W
		[0]	Synchronization mode	0	JESD204B synchronization mode. The SYSREF signal resets all internal clock dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers must change, the JESD204B link goes down.	0x0	R/W
				1	Timestamp mode. The SYSREF signal does not reset internal clock dividers. In this mode, the JESD204B link and the signal monitor are not affected by the SYSREF signal. The SYSREF signal timestamps a sample as it passes through the ADC and is used as a control bit in the JESD204B output word.		
0x011	sync error report	[7]	sync error cnt clear	0	1: clear error cnt	0x0	R/W
		[6:0]	sync error cnt	0	error cnt	0x0	R
0x012	User Pattern 1 LSB	[7:0]	User Pattern 1 [7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
0x013	User Pattern 1 MSB	[7:0]	User Pattern 1 [15:8]		User Test Pattern 1 least significant byte.	0x0	R/W
0x014	User Pattern 2 LSB	[7:0]	User Pattern 2 [7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
0x015	User Pattern 2 MSB	[7:0]	User Pattern 2 [15:8]		User Test Pattern 2 least significant byte.	0x0	R/W
0x016	User Pattern 3 LSB	[7:0]	User Pattern 3 [7:0]		User Test Pattern 3 least significant bits.	0x0	R/W
0x017	User Pattern 3 MSB	[7:0]	User Pattern 3 [15:8]		User Test Pattern 3 least significant bits.	0x0	R/W
0x018	User Pattern 4 LSB	[7:0]	User Pattern 4 [7:0]		User Test Pattern 4 least significant bits.	0x0	R/W
0x019	User Pattern 4 MSB	[7:0]	User Pattern 4 [15:8]		User Test Pattern 4 least significant bits.	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01A	Output Mode Control	[7:6]	Reserved		Reserved.	0x0	R/W
		[5:4]	Converter control Bit 2 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[3:2]	Converter control Bit 1 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[1:0]	Converter control Bit 0 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
0x01B	PLL control	[7:4]	JESD204B lane rate control	0000 0001 0010 0011 0100 0101 0110	13.5~17G 8.5~13.5G 6.75~8.5G 4.25~6.75G 3.375~4.25G 2.125~3.375G 1.6875~2.125G	0x0	R/W
		[3:0]	ADC_num	0000 0001 0010	1 ADC 2 ADC 4 ADC	0x0	R/W
0x01C	PLL status	[7]	clear_loss_lock	0 1	no action clear bit[1]	0x0	R/W
		[6:2]	Reserved	0	Reserved.	0x0	R
		[1]	PLL loss of lock	1	Loss of lock sticky bit. Indicate a loss of lock has occurred at some time. Cleared by setting bit[7].	0x0	R
		[0]	PLL lock status	0 1	Not locked. Locked.	0x0	R
0x01D	JESD204B Link status	[7:3]	Reserved		Reserved.	0x0	R
		[2]	sysref_sync_done		received SYSREF signal	0x0	R
		[1]	link_ready		PMA FSM reset done	0x0	R
		[0]	tx_ready		clk_char&clk_samp reset done.	0x0	R
0x01E	pdiv/debug_ctrl	[5]	Reserved	0	Reserved.		
		[5]	Reserved	0	Reserved.		
		[4]	Reserved	0	Reserved.		
		[3:0]	debug_sel		debug pin select control	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01F	DCM	[7]	Reserved	0	Reserved.		
		[6:0]	DCM	0000000 0000001 0000010 ..... 1111110 1111111	Decimation ratio = 1. Decimation ratio = 2. Decimation ratio = 3. ..... Decimation ratio = 127. Decimation ratio = 128.		
0x020	JESD204B Link Control 1	[7]	Standby mode	0 1	Standby mode forces zeros for all converter samples. Standby mode forces code group synchronization (K28.5 characters).	0x0	R/W
		[6]	Tail bit(t) PN	0 1	Disable. Enable.	0x0	R/W
		[5]	Syncb_error_disable	0 1	Subclass 1 or Subclass 2 receiver devices shall indicate the detection of such an error by activating the SYNC~ signal for exactly 2 frame periods. Disable.	0x0	R/W
		[4]	Lane synchronization	0 1	Disable FACI uses /K28.7/. Enable FACI uses /K28.3/ and /K28.7/.	0x1	R/W
		[3:2]	ILAS sequence mode	00 01 11	Initial lane alignment sequence disabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence enabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence always on test mode. JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.	0x1	R/W
		[1]	FACI	0 1	Frame alignment character insertion enabled (JESD204B Section 5.3.3.4). Frame alignment character insertion disabled. For debug only (JESD204B Section 5.3.3.4).	0x0	R/W
		[0]	Link control	0 1	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNC~ signal. JESD204B serial transmit link powered down (held in reset and clock gated).	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x021	JESD204B Link Control 2	[7:6]	SYNCINB± pin control	0 10 11	Normal mode. Ignore SYNCINB± (force CGS). Ignore SYNCINB± (force ILAS/user data).	0x0	R/W
		[5]	SYNCINB± pin invert	0 1	SYNCINB± pin not inverted. SYNCINB± pin inverted.	0x0	R/W
		[4]	Long transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.	0x0	R/W
		[3]	Short transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.2) sent on all link lanes.	0x0	R/W
		[2]	8-bit/10-bit bypass	0 1	8-bit/10-bit enabled. 8-bit/10-bit bypassed (most significant 2 bits are 0).	0x0	R/W
		[1]	8-bit/10-bit bit invert	0 1	Normal. Invert a, b, c, d, e, f, g, h, I, and j symbols.	0x0	R/W
		[0]	link standby	0 1	Normal mode Link standby mode, clock is on, only transmit K28.5 code.	0x0	R/W
0x022	JESD204B Link Control 3	[7:6]	Checksum mode	0 1 10 11	Checksum is the sum of all 8-bit registers in the link configuration table. Checksum is the sum of all individual link configuration fields (LSB aligned). Checksum is disabled (set to zero). For test purposes only. Unused.	0x1	R/W
		[5:4]	Test injection point	0 1 10	N' sample input. 10-bit data at 8-bit/10-bit output (for PHY testing). 8-bit data at scrambler input.	0x0	R/W
		[3:0]	JESD204B test mode patterns	0 1 10 11 100 101 110 111 1000 1110 1111	Normal operation (test mode disabled). Alternating checkerboard. 1/0 word toggle. 31-bit pseudorandom number (PN) sequence: x31 + x28 + 1. 23-bit PN sequence: x23 + x18 + 1. 15-bit PN sequence: x15 + x14 + 1. 9-bit PN sequence: x9 + x5 + 1. 7-bit PN sequence: x7 + x6 + 1. Ramp output. Continuous/repeat user test. Single user test.	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x023	JESD204B Link Control 4	[7:4]	ILAS delay	0 1 10 11 100 101 110 111 1000 1001 1010 1011 1100 1101 1110 1111	Transmit ILAS on first LMFC after SYNCINB± deasserted. Transmit ILAS on second LMFC after SYNCINB± deasserted. Transmit ILAS on third LMFC after SYNCINB± deasserted. Transmit ILAS on fourth LMFC after SYNCINB± deasserted. Transmit ILAS on fifth LMFC after SYNCINB± deasserted. Transmit ILAS on sixth LMFC after SYNCINB± deasserted. Transmit ILAS on seventh LMFC after SYNCINB± deasserted. Transmit ILAS on eighth LMFC after SYNCINB± deasserted. Transmit ILAS on ninth LMFC after SYNCINB± deasserted. Transmit ILAS on tenth LMFC after SYNCINB± deasserted. Transmit ILAS on eleventh LMFC after SYNCINB± deasserted. Transmit ILAS on twelfth LMFC after SYNCINB± deasserted. Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted. Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted. Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted. Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.	0x0	R/W
		[3]	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode	0 1 10 11 100 101 110 111	Normal operation (link layer test mode disabled). Continuous sequence of /D21.5/ characters. Reserved. Reserved. Modified RPAT test sequence. JSPAT test sequence. JTSPAT test sequence. Reserved.	0x0	R/W
0x024	JESD204B LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multi-frame clock (LMFC) phase offset value (in frame clocks). Refer to the Deterministic Latency section.	0x0	R/W
0x025	JESD204B scrambling and number lanes (L) configuration	[7]	JESD204B scrambling (SCR)	0 1	JESD204B scrambler disabled (SCR = 0). JESD204B scrambler enabled (SCR = 1).	0x1	R/W
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)	0 1 11 ... 1111	One lane per link (L = 1). Two lanes per link (L = 2). Four lanes per link (L = 4). Eight lanes per Link (L = 16).	0xB	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x026	JESD204B link number of octets per frames (F)	[7:0]	JESD204B F configuration		JESD204B number of octets per frame (F = JESD204B F configuration + 1)	0x1	R/W
				0	F = 1.		
				1	F = 2.		
				10	F = 3.		
				11	F = 4.		
				101	F = 6.		
				111	F = 8.		
				1111	F = 16.		
0x027	JESD204B link number of frames per multiframe (K)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B K configuration		JESD204B number of frames per multi-frame (K = JESD204B K configuration + 1). Only values where F × K is divisible by 4 can be used.	0x1F	R/W
0x028	JESD204B link number of converters (M)	[7:0]	JESD204B M configuration		JESD204B number of converters per link/device (M = JESD204B M configuration).	0x0	R/W
				0	Link connected to one virtual converter (M = 1).		
				1	Link connected to two virtual converters (M = 2).		
				11	Link connected to four virtual converters (M = 4).		
				111	Link connected to eight virtual converters (M = 8).		
0x029	JESD204B number of control bits (CS) and ADC resolution (N)	[7:6]	Number of control bits (CS) per sample	0	No control bits (CS = 0).	0x0	R/W
				1	1 control bit (CS = 1), Control Bit 2 only.		
				10	2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only.		
				11	3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).		
		[5]	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)	110	N = 7-bit resolution.	0xB	R/W
				111	N = 8-bit resolution.		
				1000	N = 9-bit resolution.		
				1001	N = 10-bit resolution.		
				1010	N = 11-bit resolution.		
				1011	N = 12-bit resolution.		
				1100	N = 13-bit resolution.		
				1101	N = 14-bit resolution.		
				1110	N = 15-bit resolution.		
				1111	N = 16-bit resolution.		
0x02A	JESD204B SCV NP configuration	[7:5]	Subclass support	0	Subclass 0.	0x0	R/W
				1	Subclass 1.		
		[4:0]	ADC number of bits per sample(N')	111	N' = 8.	0xB	R/W
				1011	N' = 12.		
				1111	N' = 16.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x02B	JESD204B JV S configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0] + 1).	0xF	R
0x02C	JESD204B HD CF configuration	[7]	HD value	0 1	High density format disabled. High density format enabled.	0x1	R
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link. (CF = 0)	0x0	R
0x02D	JESD204B DID configuration	[7:0]	JESD204B Tx DID value		JESD204B serial device identification (DID) number.	0x0	R/W
0x02E	JESD204B BID configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204B serial bank identification (BID) number (extension to DID).	0x0	R/W
0x030	JESD204B LID0 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204B serial lane identification (LID) number for Lane 0.	0x0	R/W
0x031	JESD204B LID1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204B serial lane identification (LID) number for Lane 1.	0x1	R/W
0x032	JESD204B LID2 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 2 LID value		JESD204B serial lane identification (LID) number for Lane 2.	0x2	R/W
0x033	JESD204B LID3 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 3 LID value		JESD204B serial lane identification (LID) number for Lane 3.	0x3	R/W
0x034	JESD204B LID4 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 4 LID value		JESD204B serial lane identification (LID) number for Lane 4.	0x4	R/W
0x035	JESD204B LID5 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 5 LID value		JESD204B serial lane identification (LID) number for Lane 5.	0x5	R/W
0x036	JESD204B LID6 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 6 LID value		JESD204B serial lane identification (LID) number for Lane 6.	0x6	R/W
0x037	JESD204B LID7 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 7 LID value		JESD204B serial lane identification (LID) number for Lane 7.	0x7	R/W
0x038	JESD204B LID8 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 8 LID value		JESD204B serial lane identification (LID) number for Lane 8.	0x8	R/W
0x039	JESD204B LID9 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 9 LID value		JESD204B serial lane identification (LID) number for Lane 9.	0x9	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03A	JESD204B LID10 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 10 LID value		JESD204B serial lane identification (LID) number for Lane 10.	0xA	R/W
0x03B	JESD204B LID11 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 11 LID value		JESD204B serial lane identification (LID) number for Lane 11.	0xB	R/W
0x03C	JESD204B LID12 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 12 LID value		JESD204B serial lane identification (LID) number for Lane 12.	0xC	R/W
0x03D	JESD204B LID13 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 13 LID value		JESD204B serial lane identification (LID) number for Lane 13.	0xD	R/W
0x03E	JESD204B LID14 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 14 LID value		JESD204B serial lane identification (LID) number for Lane 14.	0xE	R/W
0x03F	JESD204B LID15 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 15 LID value		JESD204B serial lane identification (LID) number for Lane 15.	0xF	R/W
0x040	JESD204B Lane Assign 1	[7:4]	SERDOUT1± lane assignment		Physical Lane 1 assignment.	0x1	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1 (default).		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT0± lane assignment		Physical Lane 0 assignment.	0x0	R/W
				0	Logical Lane 0 (default).		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x041	JESD204B Lane Assign 2	[7:4]	SERDOUT3± lane assignment		Physical Lane 3 assignment.	0x3	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3 (default).		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT2± lane assignment		Physical Lane 2 assignment.	0x2	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1		
				10	Logical Lane 2 (default).		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
0x042	JESD204B Lane Assign 3	[7:4]	SERDOUT5± lane assignment		Physical Lane 5 assignment.	0x5	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5 (default).		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT4± lane assignment		Physical Lane 4 assignment.	0x4	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4 (default).		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x043	JESD204B Lane Assign 4	[7:4]	SERDOUT7± lane assignment		Physical Lane 7 assignment.	0x7	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				111	Logical Lane 7 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT6± lane assignment		Physical Lane 6 assignment.	0x6	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				110	Logical Lane 6 (default).		
				1111	Logical Lane 15.		
0x044	JESD204B Lane Assign 5	[7:4]	SERDOUT9± lane assignment		Physical Lane 9 assignment.	0x9	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1001	Logical Lane 9 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT8± lane assignment		Physical Lane 8 assignment.	0x8	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1000	Logical Lane 8 (default).		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x045	JESD204B Lane Assign 6	[7:4]	SERDOUT11± lane assignment		Physical Lane 11 assignment.	0xB	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1011	Logical Lane 11 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT10± lane assignment		Physical Lane 10 assignment.	0xA	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1010	Logical Lane 10 (default).		
				1111	Logical Lane 15.		
0x046	JESD204B Lane Assign 7	[7:4]	SERDOUT13± lane assignment		Physical Lane 13 assignment.	0xD	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1101	Logical Lane 13 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT12± lane assignment		Physical Lane 12 assignment.	0xC	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1100	Logical Lane 12 (default).		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x047	JESD204B Lane Assign 7	[7:4]	SERDOUT15± lane assignment		Physical Lane 15 assignment.	0xF	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15 (default).		
		[3:0]	SERDOUT14± lane assignment		Physical Lane 14 assignment.	0xE	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1110	Logical Lane 14 (default).		
				1111	Logical Lane 15.		
0x048	SERDOUTx± data invert	[7]	Invert SERDOUT7± data		Invert SERDOUT7± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[6]	Invert SERDOUT6± data		Invert SERDOUT6± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[5]	Invert SERDOUT5± data		Invert SERDOUT5± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[4]	Invert SERDOUT4± data		Invert SERDOUT4± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[3]	Invert SERDOUT3± data		Invert SERDOUT3± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[2]	Invert SERDOUT2± data		Invert SERDOUT2± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[1]	Invert SERDOUT1± data		Invert SERDOUT1± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[0]	Invert SERDOUT0± data		Invert SERDOUT0± data.	0x0	R/W
				0	Normal.		
				1	Invert.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x049	SERDOUTx± data invert	[7]	Invert SERDOUT15± data	0 1	Invert SERDOUT15± data. Normal. Invert.	0x0	R/W
		[6]	Invert SERDOUT14± data	0 1	Invert SERDOUT14± data. Normal. Invert.	0x0	R/W
		[5]	Invert SERDOUT13± data	0 1	Invert SERDOUT13± data. Normal. Invert.	0x0	R/W
		[4]	Invert SERDOUT12± data	0 1	Invert SERDOUT12± data. Normal. Invert.	0x0	R/W
		[3]	Invert SERDOUT11± data	0 1	Invert SERDOUT11± data. Normal. Invert.	0x0	R/W
		[2]	Invert SERDOUT10± data	0 1	Invert SERDOUT10± data. Normal. Invert.	0x0	R/W
		[1]	Invert SERDOUT9± data	0 1	Invert SERDOUT9± data. Normal. Invert.	0x0	R/W
		[0]	Invert SERDOUT8± data	0 1	Invert SERDOUT8± data. Normal. Invert.	0x0	R/W
0x050	JESD204B Checksum 0 configuration	[7:0]	lane0_chksum		Serial checksum value for Lane 0. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 0) mod 256.		R
0x051	JESD204B Checksum 1 configuration	[7:0]	lane1_chksum		Serial checksum value for Lane 1. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 1) mod 256.		R
0x052	JESD204B Checksum 2 configuration	[7:0]	lane2_chksum		Serial checksum value for Lane 2. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 2) mod 256.		R
0x053	JESD204B Checksum 3 configuration	[7:0]	lane3_chksum		Serial checksum value for Lane 3. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 3) mod 256.		R
0x054	JESD204B Checksum 4 configuration	[7:0]	lane4_chksum		Serial checksum value for Lane 4. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 4) mod 256.		R
0x055	JESD204B Checksum 5 configuration	[7:0]	lane5_chksum		Serial checksum value for Lane 5. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 5) mod 256.		R
0x056	JESD204B Checksum 6 configuration	[7:0]	lane6_chksum		Serial checksum value for Lane 6. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 6) mod 256.		R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x057	JESD204B Checksum 7 configuration	[7:0]	lane7_chksum		Serial checksum value for Lane 7. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 7) mod 256.		R
0x058	JESD204B Checksum 8 configuration	[7:0]	lane8_chksum		Serial checksum value for Lane 8. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 8) mod 256.		R
0x059	JESD204B Checksum 9 configuration	[7:0]	lane9_chksum		Serial checksum value for Lane 9. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 9) mod 256.		R
0x05A	JESD204B Checksum 10 configuration	[7:0]	lane10_chksum		Serial checksum value for Lane 10. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 10) mod 256.		R
0x05B	JESD204B Checksum 11 configuration	[7:0]	lane11_chksum		Serial checksum value for Lane 11. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 11) mod 256.		R
0x05C	JESD204B Checksum 12 configuration	[7:0]	lane12_chksum		Serial checksum value for Lane 12. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 12) mod 256.		R
0x05D	JESD204B Checksum 13 configuration	[7:0]	lane13_chksum		Serial checksum value for Lane 13. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 13) mod 256.		R
0x05E	JESD204B Checksum 14 configuration	[7:0]	lane14_chksum		Serial checksum value for Lane 14. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 14) mod 256.		R
0x05F	JESD204B Checksum 15 configuration	[7:0]	lane15_chksum		Serial checksum value for Lane 15. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 15) mod 256.		R
0x60	PMA fifo wr enable	[7:0]	dbg_fifo_wr[7:0]		FIFO write enable for lane 0~7		R
0x61	PMA fifo wr enable	[7:0]	dbg_fifo_wr[15:8]		FIFO write enable for lane 8~15		R
0x62	PMA fifo rd enable	[7:0]	dbg_fifo_rd[7:0]		FIFO read enable for lane 0~7		R
0x63	PMA fifo rd enable	[7:0]	dbg_fifo_rd[15:8]		FIFO read enable for lane 8~15		R
0x64	PMA fifo empty	[7:0]	dbg_fifo_empty[7:0]		FIFO empty for lane 0~7		R
0x65	PMA fifo empty	[7:0]	dbg_fifo_empty[15:8]		FIFO empty for lane 8~15		R
0x66	PMA fifo full	[7:0]	dbg_fifo_full[7:0]		FIFO full for lane 0~7		R
0x67	PMA fifo full	[7:0]	dbg_fifo_full[15:8]		FIFO full for lane 8~15		R
0x68	PMA ready	[7:0]	dbg_pma_ready[7:0]		PMA ready for lane 0~7		R
0x69	PMA ready	[7:0]	dbg_pma_ready[15:8]		PMA ready for lane 8~15		R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x6A	PMA fifo rd start	[7:0]	dbg_rd_start[7:0]		FIFO read start for lane 0~7		R
0x6B	PMA fifo rd start	[7:0]	dbg_rd_start[15:8]		FIFO read start for lane 8~15		R
0x6C	PMA fifo wr start	[7:6]	Reserved		Reserved.		R
		[0]	dbg_wr_start		FIFO write start for all lanes		R

PMA PHY Register

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x00	pll_cfg0	[7:0]	JESD204B PLL cfg0			8'b0111,0101	R/W
		[7:5]	pll_cp_itrim	011	cp current trimming bits 3'b000: 50u 3'b001:100u 3'b010:150u 3'b011:200u default 3'b100:250u 3'b101:300u 3'b110:350u 3'b111:400u		R/W
		[4:3]	pll_cp_rsv	10	cp reset voltage trimming bits 2'b00: (1-12.5%)*vrst voltage 2'b01: (1-6.25%)*vrst voltage 2'b10: vrst voltage default 2'b11: (1+6.25%)*vrst voltage		R/W
		[2:1]	pll_cp_ls	10	cp level shift voltage trimming bits 2'b00: (1+12.5%)*vls voltage 2'b01: vls voltage 2'b10: vls voltage 2'b11: (1+12.5%)*vls voltage		R/W
		[0]	pll_lock_en	1	pll lock detect enable 1'b0: disable 1'b1: enable		R/W
0x01	pll_cfg1	[7:0]	JESD204B pll cfg1			8'b1010,1010	R/W
		[7:5]	pll_lpf_rtrim	101	lpf resistor trimming bits 3'b000: 10k 3'b001: 9k 3'b010: 8k 3'b011: 7k 3'b100: 6k 3'b101: 5k default 3'b110: 4k 3'b111: 3k		R/W
		[4:3]	pll_div2_itrim	01	high speed div2 current trimming bits 2'b00: 1.6mA 2'b01: 2mA 2'b10: 2.4mA 2'b11: 2.8mA		R/W
		[2:1]	pll_div2_buf	01	high speed div2buf current trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		R/W
		[0]	RSV	0	Reserved		R/W
0x02	pll_cfg2	[7:0]	JESD204B PLL cfg2			8'b0100,0010	R/W
		[7]	pll_vco_rtrim_mannul	0	pll vco rtrim mannul trimming bit 1'b0: auto mode 1'b1: mannul mode		
		[6:2]	pll_vco_rtrim_reg	10000	pll vco rtrim code in mannul mode		
		[1:0]	pll_fbdiv<1:0>	10	pll feedback divider ratio trimming bits 2'b00: /16 2'b01: /32 2'b10: /20 default 2'b11: /40		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03	pll_cfg3	[7:0]	JESD204B PLL cfg3			8'b0001,0100	R/W
		[7]	pll_tsten	0	PLL test enable 1'b0: disable 1'b1: enable		
		[6:5]	pll_atest_sel	00	PLL analog voltage select 2'b00: no select 2'b01: select ldo voltage output 2'b10: select vcntl voltage output		
		[4:3]	pll_lock_factor	10	PLL lock detect frequency compare mask select 2'b00:16'b1111 1111 1111 1000 2'b01:16'b1111 1111 1111 0000 2'b10:16'b1111 1111 1110 0000 default 2'b11:16'b1111 1111 1100 0000		
		[2:1]	pll_lock_coarse	10	PLL lock detect frequency compare counter select 2'b00:16'd65535 2'b01:16'd4095 2'b10:16'd1023 default 2'b11:16'd255		
		[0]	RSV	0	Reserved		
0x04	pll_cfg4	[7:0]	JESD204B PLL cfg4			8'b0100,0001	R/W
		[7]	pll_vco_crs_ovrden	0	VCO code overwrite enable 1'0： disable 1'b1: enable		
		[6:1]	pll_vco_code	100000	VCO overwrite code, manual mode		
		[0]	pll_vco_ofst_en	1	ignore VCO code offset enable 1'b0: disable, VCO code with offset 1'b1: enable, ignore offset		
0x05	pll_cfg5	[7:0]	JESD204B PLL cfg5			8'0001,1001	R/W
		[7]	pll_vco_band_sel	0	VCO high band and low band select in manual mode 1'b0：select high band 1'b1: select low band		
		[6:5]	pll_vco_accuracy	00	VCO calibration period select 2b'00: 4095 default 2b'01: 1023 2b'10: 16383 2b'11: 65535		
		[4]	pll_vco_band_sel_auto	1	auto select VCO high band and low band 1'b0：manual mode 1'b1: auto mode		
		[3:2]	pll_vco_offset	10	offset of the VCO coarse tuning code setting 2b'00: -1 2b'01: -2 2b'10: +1 2b'11: +2		
		[1:0]	pll_lock_latency_sel	01	waiting time trimming when PLL in the closed loop PLL 2b'00: 65535 2b'01: 16383 default 2b'10: 4095 2b'11: 1023		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x06	rcal_cfg0	[7:0]			JESD204B RCAL cfg0	8'b0101,0110	R/W
		[7:6]	ircal50u_cal_ctl	01	current trimming for the resistor calibration block 2'b00:1mA*98% 2'b01:1mA 2'b10:1mA*1.02% 2'b11:1mA*1.04%		
		[5:4]	ircal50u_pll_ctl	01	PLL calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ircal50u_tx_ctl	01	TX calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1]	rcalenb_manual	1	resistor calibration mode 1'b0: manual mode 1'b1:auto mode		
		[0]	iref_testen	0	test enable for accurate 50u current for ADC core 1'b0: disable 1'b1: enable		
0x07	rcal_cfg1	[7:0]			JESD204B RCAL cfg1	8'b0000,0000	R/W
		[7:5]	txcal_offset	000	TX cailibration code offset 3'b000: rcal _tx[4:0]= rcal[4:0] 3'b001: rcal _tx[4:0]= rcal[4:0]+1 3'b010: rcal _tx[4:0]= rcal[4:0]+2 3'b011: rcal _tx[4:0]= rcal[4:0]+3 3'b100: rcal _tx[4:0]= rcal[4:0] 3'b101: rcal _tx[4:0]= rcal[4:0]-1 3'b110: rcal _tx[4:0]= rcal[4:0]-2 3'b111: rcal _tx[4:0]= rcal[4:0]-3		
		[4:2]	pllcal_offset	000	PLL calibration code offset 3'b000: rcal _pll[4:0]= rcal[4:0] 3'b001: rcal _pll[4:0]= rcal[4:0]+1 3'b010: rcal _pll[4:0]= rcal[4:0]+2 3'b011: rcal _pll[4:0]= rcal[4:0]+3 3'b100: rcal _pll[4:0]= rcal[4:0] 3'b101: rcal _pll[4:0]= rcal[4:0]-1 3'b110: rcal _pll[4:0]= rcal[4:0]-2 3'b111: rcal _pll[4:0]= rcal[4:0]-3		
		[1:0]	RSV	00	Reserved		
0x08	tx_cfg0	[7:0]			JESD204B TX cfg0	8'b1110,0000	R/W
		[7:6]	tx_wide_mode, tx_divbyfive	11	TX data width select 2'b00: 16 bits 2'b01: 20 bits 2'b10: 32 bits 2'b11: 40 bits		
		[5:3]	tx_drvbiastrim	100	driver bias current trimming 3'b000: -40uA 3'b001: -30uA 3'b010: -20uA 3'b011: -10uA 3'b100: +0uA 3'b101: +10uA 3'b110: +20uA 3'b111: +30uA		
		[2:0]	tx_emppre	000	TX pre-cursor setting		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x09	tx_cfg1	[7:0]			JESD204B TX cfg1	8'b1000,0000	R/W
		[7:3]	tx_termprog	10000	TX code manual		
		[2]	tx_dcc_enb	0	TX duty cycle calibration enable, active low 1'b0: enable 1'b1: disable		
		[1]	tx_termcodesel	0	TX code mode select 1'b0: auto mode 1'b1: manual mode		
		[0]	tx_termtest	0	TX term test		
0x0A	tx_cfg2	[7:0]			JESD204B TX cfg2	8'b0000,0000	R/W
		[7]	tx_tstdiven	0	TX low speed data test enable 1'b0: disable 1'b1: enable		
		[6:3]	tx_amonsel	0000	TX analog test voltage select, detail see TestMux		
		[2]	tx_pdivsel<2>	0	TX post divider by 16 when it is enabled		
		[1]	tx_prbs_en	0	TX PRBS enable 1'b0:disable 1'b1: enable		
		[0]	tx_prbs_mode	0	TX PRBS mode select 1'b0: 0101 pattern 1'b1: prbs7 pattern		
0x0B	com_cfg0	[7:0]			JESD204B COM cfg0	8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6]	com_dig_tst_sel	0	digital signal select 1'b0: select refclk for com_tstclk<0> /select fbclk for com_tstclk<1> 1'b1: select tielow for com_tstclk<0> /select cfgclk for com_tstclk<1>		
		[5:0]	com_ana_tst_sel	000000	analog signal select detail see Test Mux		
0x0C	bg_cfg0	[7:0]			JESD204B bg cfg0	8'b0101,0101	R/W
		[7:6]	ir50u_pll_ctrl	01	VBGR current of pll trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[5:4]	ir50u_buff_ctrl	01	VBGR current of buffer trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ir50u_rcal_ctrl	01	VBGR current of RCAL trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1:0]	ir50u_spare_ctrl	01	VBGR current of spare trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0D	bg_cfg1	[7:0]	JESD204B BG cfg1			8'b0110,0000	R/W
		[7:6]	bg_trimcom	01	BG voltage trimming bits 2'b00:1.193v 2'b01:1.216v 2'b10:1.24v 2'b11:1.264v		
		[5:3]	bg_trimvco	100	VCO voltage trimming bits 3'b000:1.119v 3'b001:1.144v 3'b010:1.168v 3'b011:1.193v 3'b100:1.216v 3'b101:1.24v 3'b110:1.264v 3'b111:1.288v		
		[2]	bg_safemode	0	BG safe mode enable 1'b0: normal mode 1'b1: safe mode		
		[1]	bg_testen	0	BG test enable 1'b0: disable 1'b1: enable		
		[0]	RSV	0	Reserved		
0x0E	pma_top_cfg0	[7:0]	JESD204B PMA top cfg0			8'b1000,0000	R/W
		[7:6]	pma_top_buf_itrim	10	clock buffer trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		
		[5]	RSV	0	Reserved		
		[4:0]	pma_top_clktst_sel	00000	PMA top test signal select detail see Test Mux		
0x0F	pma_top_cfg1	[7:0]	JESD204B PMA top cfg1			8'b0000,0001	R/W
		[7]	bg_pwrdn	0	BG power down enable 1'b0: normal work 1'b1: power down	.	
		[6]	pll_pwrdn	0	PLL power down enable 1'b0: normal work 1'b1: power down		
		[5:4]	RSV	000000	Reserved		
		[3]	pllck_dccfix	0	PLL Clock duty cycle calibration fixed function 1'b0: normal work 1'b1: dcc output fixed to an equal level		
		[2]	pllck_dccenb	0	PLL Clock duty cycle calibration enable, active low 1'b0: normal work 1'b1: disable PLL Clock DCC function		
		[1:0]	pllck_dcctrim	01	DCC current trimming bits 2'b00: 0.6mA 2'b01: 0.9mA 2'b10: 1.2mA 2'b11: 1.5mA		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10	adc_clk_stime	[7:0]	JESD204B ADC Clock wait time			8'b1000,0000	R/W
		[7:3]	cfg_clk_wait_time	10000	PMA reset sequence adc_clk stable time control bits: cycle = 2^adc_clk_stime 5'b00000: 1 cycles of Cfg_Clk; 5'b00001: 2^1 cycles of Cfg_Clk; 5'b00010: 2^2 cycles of Cfg_Clk; ….; 5'b10000: 2^16 cycles of Cfg_Clk; default ….; 5'b11111: 2^31 cycles of Cfg_Clk;		
		[2:0]	RSV	000	Reserved		
0x11	fsm_reset_seq	[7:0]	JESD204B FSM reset			8'b0000,0000	R/W
		[7]	top_seq_bypass	0	top sequence bypass 1'b0: normal work 1'b1: bypass		
		[6]	lnk_rdy	0	link_ready 1'b0: not ready 1'b1: link ready		
		[5]	rcal_enb	0	RCAL enable,active low 1'b0: enable 1'b1: disable		
		[4]	pll_rstb	0	PLL reset,active low 1'b0: reset 1'b1: normal work		
		[3]	tx_rstb	0	TX reset,active low 1'b0: reset 1'b1: normal work		
		[2]	rstb_d	0	MAC reset,active low 1'b0: reset 1'b1: normal work		
		[1:0]	RSV	00	Reserved		
0x12	divider_cfg	[7:0]	JESD204B divider cfg in mannual			8'b0000,0000	R/W
		[7:6]	pll_mdiv	00	mdivider select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[5:4]	tx_pdiv	00	pdivide select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[3]	div_sel	0	1'b0: pll_mdiv/tx_pdiv use fsm value 1'b1: pll_mdiv/tx_pdiv use reg 0x12 bits [7:4].		
		[2]	adcdiv1	0	predivider in adc. 0: div 2 1: div 3		
		[1:0]	adcdiv0	00	predivider in adc. 00: div 1 01: div 2 10: div 4 11: div 8		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x13	time_1us_set	[7:0]	time count for 1us			8'b1000,1010	R/W
		[7:0]	time_1us	1000,1010	timer count for 1.25us at 110MHz		
0x14	tx_pwr_cfg0	[7:0]	TX power down config			8'b0000,0000	R/W
		[7:0]	tx_pwrdn	0000,0000	TX power down 1'b0: normal work 1'b1: power down bit<7>: control lane7 ... bit<0>: control lane0		
0x15	tx_pwr_cfg1	[7:0]	TX power down config			8'b0000,0000	R/W
		[7:0]	tx_pwrdn	0000,0000	TX power down 1'b0: normal work 1'b1: power down bit<7>: control lane15 ... bit<0>: control lane8		
0x16	pll_status	[7:0]	PLL status			8'b0000,0000	R
		[7]	RSV	0	Reserved		
		[6]	pll_afc_fine_en		PLL fine tuning mode indicator 1'b0: coarse tuning process 1'b1: fine tuning process		
		[5:0]	pll_vco_ctrim		VCO band code		
0x17	rcal_code	[7:0]	RCAL code			8'b0000,0000	R
		[7:5]	RSV	00	Reserved		
		[4:0]	rcal_code		resistor calibration code		
0x20	tx_drvamp_cfg0	[7:0]	TX drvamp cfg0			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane1	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane0	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x21	tx_drvamp_cfg1	[7:0]	TX drvamp cfg1			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane3	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane2	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x22	tx_drvamp_cfg2	[7:0]	TX drvamp cfg2			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane5	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane4	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x23	tx_drvamp_cfg3	[7:0]	TX drvamp cfg3			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane7	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane6	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x24	tx_drvamp_cfg4	[7:0]	TX drvamp cfg4			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane9	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane8	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x25	tx_drvamp_cfg5	[7:0]	TX drvamp cfg5			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane11	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane10	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x26	tx_drvamp_cfg6	[7:0]	TX drvamp cfg6			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane13	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane12	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x27	tx_drvamp_cfg7	[7:0]	TX drvamp cfg7			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane15	100	TX driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane14	100	TX driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x28	tx_post_tap_cfg0	[7:0]	TX post tap cfg0			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane1	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane0	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x29	tx_post_tap_cfg1	[7:0]	TX post tap cfg1			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane3	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane2	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2A	tx_post_tap_cfg2	[7:0]	TX post tap cfg2			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane5	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane4	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2B	tx_post_tap_cfg3	[7:0]	TX post tap cfg3			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane7	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane6	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2C	tx_post_tap_cfg4	[7:0]	TX post tap cfg4			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane9	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane8	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2D	tx_post_tap_cfg5	[7:0]	TX post tap cfg5			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane11	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane10	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2E	tx_post_tap_cfg6	[7:0]	TX post tap cfg6			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane13	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane12	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2F	tx_post_tap_cfg7	[7:0]	TX post tap cfg7			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane15	000	TX post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane14	000	TX post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

10 Package Outline

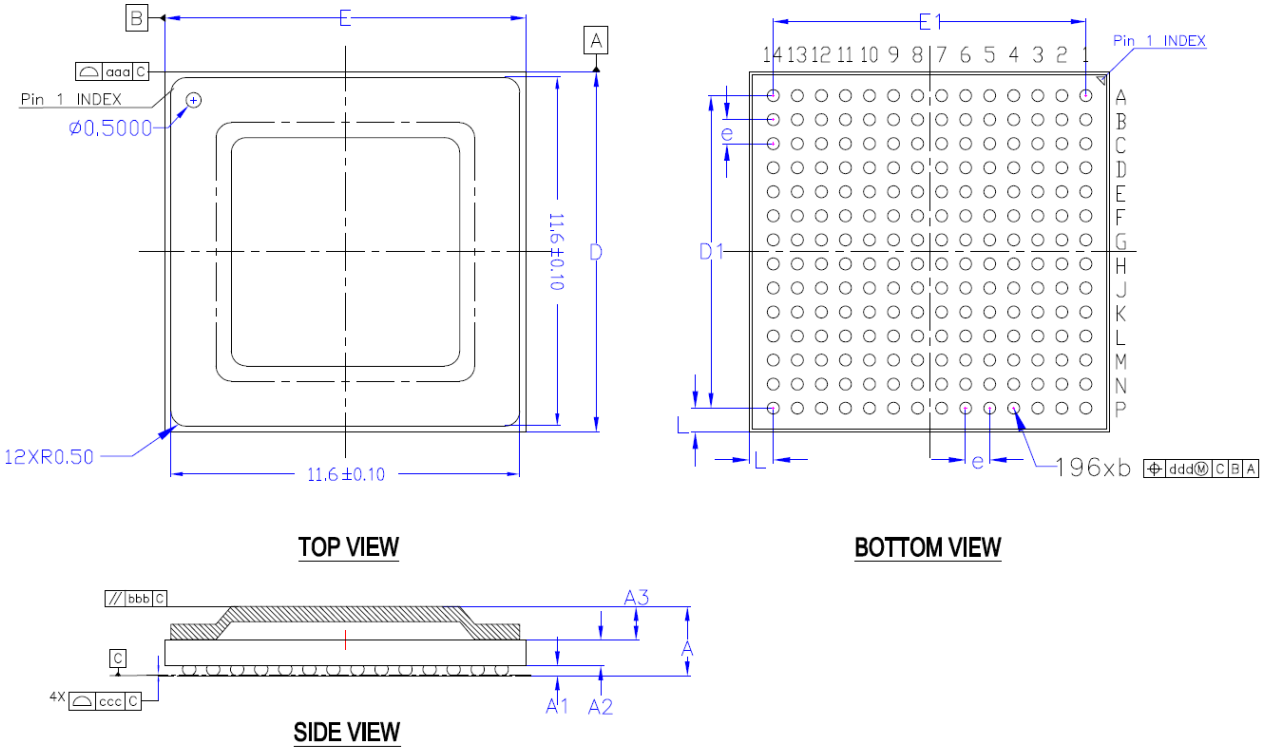


Fig. 10-1. FCBGA196 Package Dimensional Diagram

Dimensional Ref.

REF. Min.		Nom.	Max.
A	2.13	2.32	2.51
A1	0.30	0.35	0.40
A2	0.76	0.85	0.94
A3	1.07	1.12	1.17
D	11.9	12.0	12.1
E	11.9	12.0	12.1
D1	10.4 BSC		
E1	10.4 BSC		
L	0.8 REF		
e	0.8 BSC		
b	0.40	0.45	0.50
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.05		

Notes:

1. All Dimensions are in Millimeters (Angles in Degrees).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

11 Orderable Information

Model	Product Descriptions	Junction Temp	Package Description	Type
CAE2500	12b 4Gsps RF sampling ADC	-40℃ to +115℃	196 balls – Flipped Ball Matrix Package	FCBGA-196
CAE2600	12b 2Gsps RF sampling ADC	-40℃ to +115℃	196 balls – Flipped Ball Matrix Package	FCBGA-196
CAE2700	12b 1Gsps RF sampling ADC	-40℃ to +115℃	196 balls – Flipped Ball Matrix Package	FCBGA-196

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